F3974-000019

INSTALLATION AND SERVICE MANUAL

BKR 91060A

21XX MAC DISK EMULATOR SUBSYSTEM

REVISION 1.2

October 1996

Part Number 91060-90001

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LIST of EFFECTIVE PAGES

The following list provides information on the change status for this manual. Any changes issued will be indicated by additions to this list. When this manual is reprinted normally all outstanding revisions will be incorporated and the revision level of the manual will be updated to reflect such changes.

REVISION 1.0 - Original Printing - Preliminary

REVISION 1.2 - October, 1996 - Full Disk Copy Feature Added

1.1.1. PURPOSE

The purpose of this manual is to provide sufficient information for the installation, operation, programming and service of the BKR Model 91060A MAC DISK EMULATOR SUBSYSTEM.- This manual is intended for installation and service personnel experienced in with HP 21XX series computer systems. Personnel should also be familiar with the SCSI-1 (1988) Interface Operation.

The Model 91060A is a flexible microprocessor based subsystem which accepts I/O commands and data from the HP 21XX backplane, translates that information to SCSI commands and data and passes the SCSI commands and data to a SCSI drive. The subsystem consists of a HP 21XX compatible I/O PCA, a Drive select switch panel and a SCSI removable disk drive. The intent of the MAC DISK EMULATOR SUBSYSTEM is to emulate the MAC series disk controllers for the HP 7906, 7920, and 7925 Disk drives.

1.1.2. NOTES, CAUTIONS, AND WARNINGS

This manual may contain certain Notes, Cautions, and Warnings regarding the installation, use, and/or service of this equipment. Before proceeding with any installation or service of this equipment make sure you are thoroughly familiar with the contents of this manual and understand all Notes, Cautions, and Warnings. The usage of Notes, Cautions, and Warnings is as follows:

NOTE:

Notes are used to emphasize a particular aspect or item of information which should be given close attention.

CAUTION:

Cautions are used to identify certain possible errors or omissions which could cause incorrect operation or hardware damage.

WARNING:

Warnings are used to identify any condition which may cause personal injury to installation or service personnel.

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2. INTRODUCTION

This manual provides installation, operation, and service information for the BKR Model·91060A·MAC Disk Emulator Subsystem. Persons using this manual should be familiar with the HP 21XX series computer hardware and programming. In addition, to develop programs for the MAC DISK EMULATOR, knowledge of the Intel 808x series microprocessors, the SCSI-1 Interface Operation and the NEC 53C90A is necessary. The MAC DISK EMULATOR Subsystem is designed to replace older HP 21XX series Disk Drive subsystems while maintaining HP 21XX program code compatibility. The Subsystem "Emulates" the older HP Disk Drive subsystems thus allowing direct replacement without modification of existing HP 21XX programs.

The objective of the Emulator Interface Kit is to provide a modern removable, high capacity drive replacement kit for the Hewlett-Packard 7906, 7920 and 7925 14" removable cartridge drives. The replacement kit includes an interface card capable of being inserted in a Hewlett-Packard 21XX E,F Series computer which emulates the functions of the HP 13037A MAC Disk Controller in an RTE IV, RTE IVB, or RTE VI operating system environment using the HP DVR32 driver. The Emulator interface card uses the Small Computer System Interface (SCSI-1) bus for communication between the interface card and the replacement drive. The 91060A is not 100% compliant with the HP13037A Controller. Programs which make use of 13037A unique features such as the MAC disk diagnostic may not execute error free.

The MAC DISK EMULATOR SUBSYSTEM is composed of a Printed Circuit Assembly (PCA) designed to plug into the HP 21XX I/O backplane, a Subsystem Control Panel, interface cable, and one to four SCSI-1 removable disk drives.

The MAC DISK EMULATOR PCA contains an NEC V40 microprocessor and is inserted into the HP 21XX I/O Backplane. The Input, Output and Control signals from the HP 21XX Backplane are monitored by the microprocessor. Based upon the sequence of the HP 21XX I/O operations, the microprocessor may execute various functions depending upon the specific emulation requirements. The commands from the backplane may be converted into SCSI commands by the microprocessor and sent to an external SCSI disk drive over the SCSI-1 bus or may be solely processed by the microprocessor. Data to and from the HP 21XX backplane is transferred under the HP 21XX DMA to or from buffers on the PCA. Contents of the buffers are subsequently transferred to or from RAM memory under control of the V40 DMA. Data to and from the SCSI bus is also transferred under control of the V40 DMA.

The Subsystem Control Panel provides two sets of switches representing two HP Units or Drives. Each set provides octal digit thumbwheel switches for selection of emulated disk cartridges, a Format switch and upper/lower protect switches.

The MAC DISK EMULATOR SUBSYSTEM

Table 2 - Subsystem Specifications summarizes the Specifications for the MAC DISK EMULATOR.

2.1. SPECIFICATIONS

TABLE 1 - SUBSYSTEM COMPONENTS

Description	Part Number
Emulator PCA	BKR 91060-60001
Emulator Control Panel	BKR 91060-60002
Interface Cable	BKR 91060-60003
Removable Disk Drive	SyQuest Technology SQ 3270S
Removable Disk	SyQuest Technology SQ 327 270 MB
Installation and Service Manual	BKR 91060-90001

TABLE 2 - SUBSYSTEM SPECIFICATIONS

Card Dimensions	
Width	7.75 in (197 mm)
Height	8.69 in (220 mm)
Control Panel Dimensions	
Width	19.00 in (482.6 mm)
Height	3.50 in (88.9 mm)
Power Requirements	
5.1 Vdc	1.8 Amp
-2.0 Vdc	0.08 Amp
12.0 Vdc	0.01 Amp
-12.0 Vdc	0.01 Amp
Processor	
Type	NEC V40 (PD70208)
Oscillator Freq.	20 Mhz
RAM	512 Kbyte Max
ROM	512 Kbyte Max
SCSI Interface	
Specification	Conforms to SCSI-1 Standards
Controller	NCR 53C90A Advanced SCSI Controller
Backplane Interface	
Input Buffer	4 Words
Output Buffer	4 Words

3. INSTALLATION

This section provides information for setup and installation of the BKR 91060A MAC DISK EMULATOR Subsystem. This information includes installation of the PCA, installation of the Control Panel and connection of the interface cable. Installation of the SCSI Disk drives is dependent upon the specific drive used and is covered in information supplied with the drive. This section also details the setting of certain jumpers and switches on the PCA. These are used to define the specific EPROM and RAM parts installed. Table 7 - P2 Connector Pin Assignments presents the P2 Connector pin assignments.

Information is also provided for repackaging and shipment.

3.1. GENERAL

Installation of the MAC DISK EMULATOR Subsystem includes installation of the Control Panel, the Emulator I/O Card, the SCSI Disk Drives and Cable(s).

The Subsystem Control Panel is designed to be mounted in a standard 19 inch EIA electronics rack. The panel requires 3.5 Inches of vertical rack space. The panel should be located at a convenient position for the intended system operation. Actual location is limited only by cable length from the I/O card. This cable is 10 Ft. Long.

The SCSI Disk Drives are supplied in a rack mounted chassis and should also be mounted at an appropriate location, again considering cable length limitations.

The 91060A MAC DISK EMULATOR PCA is designed to be used with only the HP 21XX E and F Series computers.

3.2. CONTROL PANEL INSTALLATION

Connect the 15 Pin connector on the Emulator I/O cable, P/N 91060-60003, to the 15 pin connector on the Control Panel. Route the cable to the 21XX computer I/O Card Cage. Install the Control Panel in the rack using four mounting screws.

3.3. EMULATOR PCA INSTALLATION

CAUTION:

Before installation of the PCA into the computer backplane, verify all jumper and switch settings are correct. This section details setting the jumper plugs on the PCA. Switch settings are dependent upon the specific Firmware installed on the PCA. See the operating section for specifics on setting the switches.

WARNING:

REMOVE ALL POWER FROM THE HP 21XX COMPUTER BEFORE REMOVING OR INSTALLING ANY PCA OR I/O CABLE.

INSTALLATION

To install the MAC DISK EMULATOR PCA, determine the specific I/O slot in the 21XX backplane into which the PCA is to be installed. Remove any existing PCA. Orient the MAC DISK EMULATOR PCA such that the components face the same direction as the components on all other PCA's. Slide the PCA into the backplane and push firmly to seat the card in the backplane connector. Verify seating by observing that the extractors are at the same level as all other extractors.

3.3.1. PCA JUMPER SETTINGS

The type and size of RAM and EPROM memory parts installed on the 91060A PCA are determined by jumpers located on the 91060A PCA. A small jumper plug is used to make connection between the jumper pins as required. In addition to setting the RAM and EPROM information, jumpers are also provided to enable certain processor interrupts.

TABLE 3 - RAM JUMPER SETTINGS

	TYPE	SIZE	W3	W4
⇒	HM628128	128 Kbyte	IN	2-3
	HM62256	32 Kbyte	OUT	1-2

TABLE 4 - EPROM JUMPER SETTINGS

	TYPE	SIZE	W1	W2	W5
	27C010	1024 Kbit	IN	IN	2-3
⇒	27C512	512 Kbit	OUT	IN	1-2
	27C256	256 Kbit	IN	OUT	1-2

Table 3 - RAM Jumper Settings provides the jumper definitions for the RAM installation on the PCA. Table 4 - EPROM Jumper Settings provides the jumper definitions for EPROM installation on the PCA. Table 5 - Interrupt Jumper Settings provides the jumper definitions for interrupt inputs to the microprocessor. Jumper W11 is not used. The ⇒ symbol indicates the factory default settings.

3.3.2. EPROM SIZE

Jumpers W1, W2 and W5 are used to set the size of the EPROMs installed in sockets U46 and U47. Three sizes of EPROMs are supported, 256 Kbit, 512 Kbit and 1024 Kbit. Set the jumpers as indicated in Table 4 - EPROM Jumper Settings according to the size of EPROM being installed. If two EPROMs are installed, they must be the same size. If one EPROM is installed, it must be installed in socket U47. EPROM access time (speed) must be 150 nsec or less.

CAUTION:

When installing 28 pin EPROMs (256 and 512 Kbit parts) in 32 pin sockets, place the parts so that pin 14 of the EPROM mates with pin 16 of the socket. Pin 1 of the EPROM will then be inserted into pin 3 of the socket.

3.3.3. RAM SIZE

Jumpers W3 and W4 select the size of the static RAM parts installed in sockets U44 and U45. Two sizes of static RAM are supported, 256 Kbit and 1024 Kbit. Set jumpers W3 and W4 as directed by Table 3 - RAM Jumper Settings, to match the part being installed. Also, see the caution above when installing a 28 pin part in a 32 pin socket. If two RAM parts are installed they must both be the same size. If only one RAM is installed, install the part in socket U44. RAM access time (speed) must be 120 nsec or less.

3.3.4. INTERRUPT ENABLES

Jumpers W6 through W10 select interrupt response conditions for the microprocessor. These jumpers route signals from the I/O backplane to the microprocessor interrupt inputs. Jumpers should be installed as required by the firmware. For the MAC DISK EMULATOR install the jumpers as shown Table 5 - Interrupt Jumper Settings.

TABLE 5 - INTERRUPT JUMPER SETTINGS

Jumper	Position (default)	Usage
W6	Out	Control F/F Interrupt
W7	In	Input Data Ready Interrupt
W8	Out	Command F/F Interrupt
W9	Out	Output Ready Interrupt
W10	Out	EDT Interrupt

3.3.5. HP21XX POWER SUPPLY VERIFICATION

CAUTION

Correct operation of the MAC DISK EMULATOR PCA requires the 5.0 Vdc supplied to the PCA to be at least 5.00 Volts. After installation of the PCA into the 21XX backplane, apply power to the HP21XX and verify the HP21XX 5.0 Volt supply is set to provide at least 5.0 Volts as measured on pin A35 of the MAC DISK EMULATOR PCA P2 Connector. If adjustment is required, refer to the appropriate HP documentation for power supply adjustment.

3.3.6. CABLE INSTALLATION

Connect the 91060-60002 I/O Cable P2 connector to the edge of the MAC DISK EMULATOR PCA. Verify the orientation of the P2 connector, the cable end of the connector should be oriented away from the LEDs on the PCA. Push the P2 connector onto the card-edge connector and verify proper seating.

3.4. SCSI DRIVE INSTALLATION

Mount the SCSI Disk Drive(s) in the rack using appropriate mounting hardware. Slides are not required but may be used to assist in service. Route the remaining cable (SCSI I/O Cable) to the SCSI disk drive and connect. If more than one disk drive is installed, verify a chaining cable is installed between drives. Also verify proper installation of SCSI termination resistors.

NOTE:

Proper termination of the SCSI Bus must be maintained to assure data reliability. Verify each end of the Bus is terminated and that no termination's are installed on any intermediate devices. Only one device should supply termination power. Remove fuse F1 from the 91060A PCA if any other device on the Bus supplies Termination Power.

3.4.1. SCSI DRIVE SETUP

The MAC Emulator supports up to two HP drives/Units using up to four SCSI removable cartridge drives. Refer to the SyQuest SQ-3270 Installation Manual for the location of the SCSI ID jumpers and the termination resistors. When installing the drives, the SCSI ID jumpers need to be set for each drive installed. A drive with SCSI ID set to 0 is always required and becomes the primary drive for HP Unit 0. This drive is associated with the Drive A switch section on the Control Panel. It is recommended this drive be connected on the SCSI bus cable as the final drive on the cable and that the termination resistors be installed in this drive.

The remainder of these instructions depend on the drive configuration desired. The Emulator can control up to four SCSI drives acting as 7906, 7920 or 7925 HP drives. However, only two HP Units (drives) can be controlled from one emulator card. The 7920 and 7925 emulations are only supported with a single SCSI drive. HP Units emulating the 7906 drive can be set up using one or two SCSI drives to retain the removable cartridge independence of the HP drive.

A 7906 Unit can be configured with a single SCSI drive, however, if this is done, the removable platter feature of the 7906 is lost. Although data can be written to seven different removable platters for a total data space of 80 Mbytes, there is no way to separate data written to the fixed platter from the data written to any of the seven removable platters. When the data on the removable platters is removed, the data on the fixed platter goes with them. With two SCSI drives assigned to a 7906 unit, the platters accessed using switch numbers 10 through 17 can be removed from the secondary drive without disturbing the data on the fixed platter on the primary drive. Table 6 - Drive Configurations lists the possible combinations.

TABLE 6 - DRIVE CONFIGURATIONS

	Configuration	Primary Drive SCSI ID	Secondary Drive SCSI ID	PCA DIP SWITCH ON
1	HP Unit 0 as a 7906 with one SCSI drive	0	N/A	
2	HP Unit 0 as a 7906 with two SCSI drives	0	1	SW1.7
3	HP Unit 1 as a 7906 with one SCSI drive	2	N/A	
4	HP Unit 1 as a 7906 with two SCSI drives	2	3	SW1.8
5	HP Unit 0 as a 7920 or 7925	0	N/A	
6	HP Unit 1 as a 7920 or 7925	2	N/A	

When the two HP Units are both configured as single drive 7906's, another option known as the Alternate 7906 configuration is available. Setting the Drive A digit switches between 10 and 17 allows the Drive B 7906 to be used in the same manner as the Unit 0 secondary drive. Refer to section 4.3.2 for more detail about the operation of this configuration.

Connect a SCSI 50 pin ribbon cable with two IDE pin headers to both drives (observe pin 1 polarity). At least one end of the cable must be terminated in a 50 pin *Micro Ribbon* female connector for connection to the male SCSI connector of the Emulator Interface cable.

Switch 7 of the PCA DIP switch must be set ON if the HP Unit 0 7906 secondary drive (SCSI ID 1) is installed. PCA DIP Switch 8 is set ON if the HP Unit 1 7906 secondary drive (SCSI ID 3) is installed. In all other instances, these switches are set to the OFF position.

3.5. STORAGE AND SHIPMENT

The MAC DISK EMULATOR PCA uses static sensitive CMOS devices. Caution must be used when handling and shipping the PCA to prevent damage from static discharges. Shipment of the PCA must be done in approved static control bag and containers. Assure a minimum of 2 inch (5 cm) packing around the PCA when packaging for shipment. If possible, retain and reuse the original shipping material.

TABLE 7 - P2 CONNECTOR PIN ASSIGNMENTS

PIN	Component Side - A -	Circuit Side - B -
1	SD0	GROUND
2	SD1	GROUND
3	SD2	GROUND
4	SD3	GROUND
5	SD4	GROUND
6	SD5	GROUND
7	SD6	GROUND
8	SD7	GROUND
9	SDP	GROUND
10	TERMPWR	TERMPWR
11	ATN	GROUND
12	BSY	GROUND
13	ACK	GROUND
14	SRST	GROUND
15	MSG	GROUND
16	SEL	GROUND
17	CD	GROUND
18	REQ	GROUND
19	SIOI	GROUND
20	GROUND	GROUND
21	OUT0	OUT1
22	OUT2	OUT3
23	OUT4	OUT5
24	OUT6	OUT7
25	BIO0	BIO1
26	BIO2	BIO3
27	BIO4	BIO5
28	BIO6	BIO7
29		
30	LED0	LED1
31	LED2	LED3
32	LED4	LED5
33	LED6	LED7
34		
35	VCC	VCC
36		
37		
38		
39	SERIAL IN	SERIAL OUT
40	GROUND	GROUND

4. EMULATOR OPERATION

4.1. INTRODUCTION

The BKR 91060 MAC Emulator card has the capability to replace a Hewlett Packard 13037A MAC Controller connected to one or two 7906, 7920 or 7925 drives provided the card is connected to one or more removable SCSI drives of adequate capacity. Actual operation depends on the type of drive selected. The HP software is normally unaware of the presence of the 91060 card. However, the firmware does not support track sparing operations or low level formatting. These features are performed by the SCSI drive internal operating firmware. The choice of drive emulation is selected by performing cartridge initialization as described later in this document. The drive type identifier is stored on the SCSI cartridge in the Vendor ID page. All emulator testing has been performed using SyQuest 3270 Removable SCSI Drives. While the SCSI-I specification supports up to 8 devices on the bus including the controller, the 91060 is limited to four drives with SCSI ID's 0 through 3. To assist in identification of the different items in this document, references to HP drives are made using the terms Unit 0 and Unit 1 or as Drive A or Drive B, respectively, when referring to the nomenclature printed on the Control Panel. When referring to one of the SCSI drives, the terms used are Drive 0 through Drive 3. This allows the simpler term to be used without having the repeatedly state HP Drive or SCSI Drive. Along the same line of thought, HP cartridges or disk packs are referred to as platters whether referring to a 7906 removable cartridge, the 7906 fixed platter, or a 7920 or 7925 disk pack. The term cartridge is only used to refer to the SyQuest SQ327 SCSI cartridge as a whole which may hold the data for more than one HP platter/pack.

NOTE

Setting the mechanical write protect device on the SyQuest cartridge to the *read only* position as a protect mechanism is unsupported by the 91060. It prevents **all** access to the cartridge. A cartridge so disabled is handled as if the cartridge were not installed in the drive. Use the Control Panel Upper and Lower Protect Switches.

4.2. CONTROL PANEL OPERATION

The Drive A and Drive B switch groups on the Control Panel apply to HP Unit 0 and HP Unit 1 respectively. The Drive A and Drive B digit switches are set to select the current active platter for the respective drive/HP Unit. A value of 00 is illegal for 7906 type drives, but is valid for 7920 or 7925 drives.

Values greater than the supported number of platters for the drive type are also invalid.

WARNING

When using the control panel under the RTE operating system, it is imperative any LU's physically located on a platter referenced by the switch panel be

DISMOUNTED
before changing any of the drive switches!

The operating program must be **rebooted** whenever the primary drive cartridge is changed, or when the primary drive switch is changed and the drive type in use is either a 7920 or a 7925.

When the drive type is 7920 or 7925, the Lower Protect Switch is used as the READ ONLY switch. The Upper Protect Switch is not used when these drive types are in operation.

4.3. DRIVE CONFIGURATIONS

There are four different drive configurations supported. They are designated as the 7906 Basic, 7906 Alternate, 7920 and 7925. The 91060 supports either one or two HP Units known as Drive A and Drive B. The SCSI drives must be assigned SCSI IDs of 0 through 4. The HP Unit 0 primary drive must be set to SCSI ID 0 and the HP Unit 1 primary drive set to SCSI ID 2 regardless of the drive type being emulated. With the exception of the 7906 Alternate, an HP Unit may be any one of the following configurations.

4.3.1. 7906 BASIC

The 7906 is a 20 megabyte drive with four heads, 411 cylinders and 48 sectors per head per cylinder position (track). The capacity is divided between a fixed platter and a removable platter. Heads 0 and 1 access the removable cartridge. The Control Panel Drive X digit switch settings 01 through 07 control access to seven separate removable platters on the primary drive. For 7906 drive type configurations, a second SCSI drive may be added with a SCSI ID of primary ID + 1. This increases the number of on-line removable platters from 7 to 15 using digit switch settings of 10 through 17. Using this configuration makes it possible to physically separate the data recorded on the fixed platter from that recorded on the removable platter. This provides the flexibility normally obtained using the HP 7906. The platter accessed on the secondary drive as platter 10 becomes the fixed platter if inserted in a primary drive.

4.3.2. 7906 ALTERNATE

This configuration option is available only when for the 7906 drive type. This option permits accessing a two SCSI drive subsystem as either two single drive 7906 Basic HP Units or as one 7906 two SCSI drive HP Unit. If the SCSI drives with ID's 0 and 2 both contain mounted 7906 type cartridges and the Drive A switch is set to 10 or higher when the 21XX Preset switch is active and pressed, the Interface will initialize to the 7906 Alternate Configuration. This means the up to eight platters located on the cartridge in Drive 2 are accessible through Unit 0 when Drive A switches are set to 10 through 17. This configuration must be selected **prior to starting the program** because it is initialized by pressing the 21XX Preset switch with the 21XX is in the *halt* state. The Drive B switches are disabled in this configuration. This feature is available *only* when the drive type is 7906 and only on Drive A!,Both Drive 0 and Drive 2 must contain mounted 7906 initialized cartridges when the PRESET switch is pressed.

4.3.3. 7920

With a 7920 type cartridge installed, up to five 7920 platters are available through the Control Panel Drive X digit switch settings of 0 through 4. **The operating system must be re-booted whenever the drive switch is changed.** Data cannot be directly transferred between one 7920 platter and another on the same cartridge. The Drive X Lower Protect switch is used to provide READ ONLY protection for the accessible platter on the cartridge. The Upper Protect switch in not used.

4.3.4. 7925

With a 7925 type cartridge installed, two 7925 platters are available through the Control Panel Drive X digit switch settings of 0 and 1. **The operating system must be re-booted whenever the drive switch is changed.** Data cannot be directly transferred between one 7925 platter and another on the same cartridge. The Drive X Lower Protect switch is used to provide READ ONLY protection for the accessible platter on the cartridge. The Upper Protect switch in not used.

4.4. CARTRIDGE INITIALIZATION

The SyQuest Cartridge initialization function is used to write an HP drive type signature to a SQ3270 cartridge and set all the data sectors and track protect bits associated with a platter to zero. It is performed using only the Drive A primary drive and the Control Panel. The 21XX must be in a halted state to initialize a cartridge. Two operations are involved to fully initialize a SyQuest Cartridge for use as one of the HP drive types.

The first operation performed writes the desired drive type to the cartridge's vendor ID page and set the contents of the platter/pack 0 data and protect blocks to all zeros. Once the drive type for the cartridge is successfully stored, any platter on the cartridge can be initialized to all zeros. This is the equivalent of using the HP FORMAT program on the platter. The HP FORMAT program is not supported on the 91060 Emulator.

WARNING

Failure to set the sectors used by a platter to zeros before attempting to use the platter in an RTE environment can produce unpredictable results!

4.4.1. CARTRIDGE INITIALIZATION SETUP

The cartridge initialization feature is enabled by setting the PCA dip switch switches 1 and 6 to the ON position. Switches 2, 3, and 4 must be set OFF. Switches 5, 7, and 8 are *don't cares* for this procedure. If the PCA dip switches are not set as specified above, the Control Panel switch settings which follow are treated as illegal values. Use of the DIP switches permits disabling cartridge initialization operations from the Control Panel in situations where it would be undesirable. Cartridges must be initialized using the Drive A primary drive. The 21XX must have power applied and be in the *halt* state. Even though the Drive B switches are used in these processes, the physical presence of a Drive B is not required.

4.4.2. INITIALIZING A CARTRIDGE TO A DRIVE TYPE

To initialize a SyQuest cartridge to hold data for a specific HP Drive type, the following steps are required:

1. Set the PCA dip switch as above.
2. Insert a cartridge in the Drive A primary drive and bring the drive to the ready condition by moving the cartridge mount lever to the right until it latches in place. Wait for the drive indicator LED to change to GREEN indicating the cartridge is mounted.
3. Set the Drive B digit switches to 77.

4. Set the Drive A FORMAT switch ON and both protect switches OFF
5. To initialize the cartridge to a drive type, set the Drive A digit switches as follows:
6. For a 7906 set switches to 76
   For a 7920 set switches to 72
   For a 7925 set switches to 75
7. Press the 21XX PRESET switch
8. Observe the drive indicator changes from green to orange. When the initialization is complete, the drive indicator will change back to GREEN. At this time the PCA LEDs start flashing between ON-OFF-ON-OFF and OFF-ON-OFF-ON.
9. Set both the Drive A and Drive B digit switches to 01.
10. Observe the PCA LEDs flash between ON-OFF-OFF-ON and OFF-ON-ON-OFF.
11. Press the 21XX PRESET switch.
12. Observe the PCA LEDs process through the start-up sequence and end with the LEDs set to OFF-OFF-OFF-ON.

This completes the platter 0 type setting and initialization for the Cartridge.

4.4.3. PLATTER INITIALIZATION

To initialize the remaining platters on the cartridge or to re-initialize any platter (the disk type remains the same) the following steps are required.

1. Set the PCA dip switch as stated above.
2. Insert the cartridge in Drive A primary drive and bring the drive to the ready condition by moving the cartridge mount lever to the right. Wait for the drive indicator LED to change to GREEN indicating cartridge is mounted.
3. Set the Drive B digit switches to 76.
4. Set the Drive A FORMAT switch ON and both protect switches OFF
5. To initialize (or re-initialize) a platter, set the Drive A digit switches as follows:
   For Platter 0 60
   For Platter 1 61
   etc. where the platter number is below the highest platter number for the drive type
6. Press the 21XX PRESET switch
7. Observe the drive indicator changes from green to orange. When the initialization is complete, the drive indicator will change back to GREEN. At this time the PCA LEDs start flashing between ON-OFF-ON-OFF and OFF-ON-OFF-ON.
8. Set both the Drive A and Drive B digit switches to 01.
9. Observe the PCA LEDs flash between ON-OFF-OFF-ON and OFF-ON-ON-OFF.
10. Press the 21XX PRESET switch.
11. Observe the PCA LEDs process through the start-up sequence and end with the LEDs set to OFF-OFF-OFF-ON.

Platter initialization is complete.

During power-on startup, the PCA LEDs are lighted in the following sequence:

CPU INIT	ON	OFF	OFF	OFF
CPU INIT COMPLETE	OFF	ON	OFF	OFF
PROGRAM INIT	ON	ON	OFF	OFF
PROG INIT COMPLETE	OFF	OFF	OFF	ON

Normal operation proceeds from the PROG INIT COMPLETE state.

4.5. FULL CARTRIDGE COPY FUNCTION

Included in firmware version 1.10 of the BKR 91060 MAC Controller Emulator is the capability to copy all HP 79XX platters on a cartridge to a second cartridge. This feature is a block by block copy and only copies entire cartridges, i.e. all eight 7906 platters, all five 7920 platters or both 7925 platters. Selective platter copying is not an option.

Copying is always performed from the B drive to the A drive. It is suggested the source cartridge be hardware protected by setting the cartridge hardware protect device, located on the underside of the cartridge, to the write protect position to prevent inadvertant writing to the master cartridge.

WARNING
A cartridge CANNOT be booted with the protect device in this position.

4.5.1. Theory of Full Cartridge Copy Operation

The cartridge in the A drive is set to the type of the B drive cartridge and all relevant blocks are transferred. While the copy process is proceeding normally, the card LEDs will sequence from 1 to 4. At the conclusion of the copy process, the Drive A load lever is ejected and the LED pattern indicates *SUCCESS*. (See LED codes below.) Should an error occur during the copy process, both load levers are ejected. The type of error is displayed by the card LEDs.

4.5.2. Procedure for use of the Full Cartridge Copy Function.

The copy function requires the DIP switches on the card be set to the FORMAT cartridge setting. The DIP switch is located on the right as the card is withdrawn from the backplane. To set the DIP switches:

1. Turn OFF power to the HP 2100
2. Remove the cable from the MAC Controller PCA.
3. Using the extractors, remove the PCA from its I/O slot.
4. Set switches 1 and 6 ON
5. Set switches 2, 3, & 4 OFF.
6. Normally switches 7 & 8 are ON. Switch 5 is unused and normally set OFF.
7. Return the PCA to its slot in the 2100 backplane and replace the cable on the edge connector.
8. Restore power to the 2100.

4.5.2.1.Copying a Cartridge

1. Insert the source (master) cartridge in the B Drive (SCSI address 2) and latch the load lever.
2. Insert the target cartridge in the A drive (SCSI address 0) and latch the load lever.
3. Wait until both drive indicators indicate the cartridge is loaded.

WARNING

All data previously stored on the target cartridge is destroyed by the copy operation.

4. On the MAC Emulator Control Panel
   a) Set the B Drive thumb wheel switches to 66.
   b) Set the B Drive format switch to OFF
   c) Set the two B Drive protect switches ON.
   d) Set the A Drive format switch to ON.
   e) Set the two A Drive protect switches to OFF.
   f) Set A Drive thumb wheel switches to 33 to copy (faster) or 36 to copy and verify the cartridge.
5. Press the HP-2100 *PRESET* switch to start the copy operation.
6. Observe the drive indicators on both drives show activity.

4.5.2.2.Successful Transfer

At the conclusion of a successful transfer, the Drive A load lever is ejected. The copy function may be terminated or another target cartridge loaded and copied to.

- To terminate the copy process:
  1. Restore the two drive thumb wheel switches to 01.
  2. Turn OFF the Drive A format switch.
  3. Press the 2100 *PRESET* switch.

The Drive B cartridge is spun down and the load lever is ejected. To boot RTE, insert and load a bootable cartridge in Drive A and proceed with the normal boot procedures.

- To copy another cartridge from the cartridge currently installed in Drive B:
  1. Remove the just copied cartridge from Drive A
  2. insert a new cartridge and latch the Drive A load lever.
  3. Wait for the green ready indicator on Drive A. (Drive B's indicator should still be green.)
  4. Press the 2100 *PRESET* switch to initiate the copy process.

4.5.2.3.Error During Transfer

If an error occurs during the copy process, the load levers of both drives are ejected. The type of error as listed in the LED Codes below is displayed by the card LEDs.

- To restart the copy:
  1. Latch the load levers on both drives.
  2. Restore the two drive thumb wheel switches to 01.
  3. Press the *PRESET* switch.
  4. Return to the copy sequence beginning at step 3 in Section 4.5.2.1 above.

- To terminate the copy process:
  5. Restore the two drive thumb wheel switches to 01.
  6. Turn OFF the Drive A format switch.
  7. Press the *PRESET* switch.

This terminates the copy process. If the copy process is terminated prior to completion, the target cartridge may be unusable until re-initialized or a successful copy to the cartridge is performed.

4.5.3. FULL CARTRIDGE COPY LED CODES

The LED indicators located at the rear edge of the Interface Card in the hp 2100 are numbered left to right from one to four. The pattern is an alternating one with the indicated LEDs being ON with the remaining LEDs OFF followed by the reverse. The codes that may be displayed during the copy process are shown in Table 8 - Full Cartridge Copy LED Codes

TABLE 8 - FULL CARTRIDGE COPY LED CODES

LED	Description
1	Error reading from the Source Drive.
2	Error writing to the Target Drive
4	Error reading or writing the protected tracks blocks
8	Error during Data Compare
1 & 2	Error reading from the Target Drive
1 & 4	SUCCESSFUL Copy occurred
1 & 8	Waiting for both drive thumb wheel switches to be returned to 01 and Drive A format switch to OFF.

5. THEORY OF OPERATION

This section describes the theory of operation of the 91060A Emulator. Sufficient information is provided for understanding the principals of operation of the Emulator. The reader is expected to be familiar with micro-processors and have specific knowledge of the Intel 808x series processors, the SCSI-1 Interface Specification, and the NCR 53C90A Advanced SCSI Controller. In addition, the reader must be familiar with the 21XX series computers and the design of 21XX I/O cards.

This section provides information on both the Hardware theory and Firmware operation. Sections 5.1 through 5.5 describe the operation of the hardware. These sections provide generic emulator descriptions as well as information specific to the operation of the MAC DISK EMULATOR. Sections 5.6 through 5.7 describe the MAC EMULATOR firmware operation.

5.1. HARDWARE DESIGN

The 91060A MAC DISK CONTROLLER Emulator is designed using the NEC V40 processor with 256 Kbytes of RAM and 64 Kbytes of ROM located on the interface card. The SCSI interface is implemented using the NCR 53C90A Advanced SCSI Controller (ASC) chip. This chip provides for an 8 bit SCSI-2 interface capability. Data transfer over the SCSI bus can achieve up to 3 MBytes/sec. As a practical matter, final data transfer speed is limited by the read/write rate of the drive itself and is a function of the number of physical sectors per track and the rotation rate and has little to do with the burst rate of either the SCSI bus or the 21XX backplane transfer rate. Multiple internal cache buffers are used to limit the number of SCSI accesses required to transfer data.

Figure 1- MAC Disk Emulator Block Diagram provides an overall block diagram of the BKR 91060A Subsystem. **Figure 2 - MAC Emulator** PCA Block Diagram presents a block diagram of the Emulator PCA.

5.2. SUBSYSTEM HARDWARE

The BKR 91060A consists of three major items of hardware, the EMULATOR PCA, the Control Panel and the SCSI-1 Removable Disk Drive(s).

The Control Panel provides the operator interface to the MAC DISK EMULATOR subsystem and provides selection data to the EMULATOR PCA. Since the Emulator provides significantly more storage capacity than the original HP drives, multiple 'removable' cartridges are emulated. The Control Panel digit switches provide the method for platter/pack changingon a mounted cartridge.

Two sets of switches on the Control Panel allow selection of multiple cartridges and emulation of two HP disk drive units. The Drive A switches control the emulation of HP Unit 0 and the Drive B switches control emulation of HP Unit 1. The Format and Upper/Lower Protect switches provide the same functionality as those found on the HP Disk Drives.

Figure 3 - BKR 91060 Control Panel Wiring details the wiring of the Control Panel.

The BKR 91060-60001 Emulator PCA provides the primary emulation functions and is described in detail in the following sections.

5.3. PROCESSOR SECTION

The Emulator PCA is controlled by an NEC V40™ microprocessor. The V40 is a highly integrated low power CMOS 16 bit microprocessor. A number of peripheral circuits are integrated within the CPU to reduce the required external logic. The peripherals included in the V40 are a PIC (Programmable Interrupt Controller), a CTC (Counter-Timer-Controller), a DMA, (Direct Memory Access Unit), and a SIO, (Serial Input Output unit). The V40 uses an external 20 bit address bus and multiplexed 8 bit data bus allowing direct addressing of 1·MBYTE memory. The V40 is instruction set compatible with the Intel 808x series processors. Programs may be developed using the same programming tools. The Emulator PCA contains four 32 pin sockets, two sockets (U44 and U45) for RAM and two sockets (U46 and U47) for EPROM. The RAM memory is designed for static byte-wide memory of either 32 Kbytes or 128 Kbytes each. The RAM memory addresses are controlled by jumpers W3 and W4. The RAM sockets (U44 and U45) may be configured for 128 Kbyte Parts (Hitachi HM628128L-12). or for 32 Kbyte Parts (HM62256L-12).

Jumpers W1, W2 and W5 control the addressing of the EPROM sockets and allow selection of 32 Kbyte, 64 Kbyte, or 128 Kbyte EPROMs. Socket U47 is always addressed as the highest addressed EPROM and must contain the Power On / Restart jump instruction at FFFF:0. The PAL U43 contains the memory address decoding logic for both the EPROM and RAM socket sets.

The V40 reset input is activated (ground true) on power up. The receipt of the POPIO signal from the backplane normally resets a 21XX series I/O PCA. For the SCSI Emulator PCA, the POPIO signal is stretched by U38B and is used to generate a processor interrupt (INT. 7). The three interrupt lines INT4, INT5 and INT6 to the V40 PIC may be configured to provide interrupts to the processor based on the actions of the I/O Backplane. The functions generating these interrupts are selected by jumpers W6 through W10. Only INT 4 is used by the 91060A Emulator firmware.

The Serial Data Unit of the V40 is connected to the P2 connector through the RS232 level converter U48. The serial port is normally used for debug purposes. PAL U42 contains decode logic for the V40 I/O instructions. All non processor I/O is decoded with this PAL starting at I/O address 8000h. LED's DS1 - DS4 provide the programmer with a means to display system status. Switches SW1-1 to SW1-8 are also provided for use by the programmer to select specific operating conditions. The LEDs are lighted by writing to the lower four bits of port 8000h. The switches may be read by an input instruction at port 8000h (**Note:** On = 0).

5.4. SCSI SECTION

The SCSI section provides an interface to the Small Computer System Interface (SCSI) bus. The SCSI bus is designed for communications with external SCSI compatible peripheral devices. U55, an NCR 53C90A, is the SCSI controller and provides SCSI-I bus control and handshake logic. SCSI bus line drivers and receivers are integrated into the controller and operate in a single ended mode. The 53C90A is programmed from the V40 using normal I/O instructions. Data is transferred directly between RAM memory and the SCSI bus under control of the V40 DMA Channel 0.

5.5. BACKPLANE I/O SECTION

The Backplane I/O section consists of three major subsections, Flag/Control, Data Input, and Data Output. The MAC Disk Controller interface uses non standard Flag and Control logic circuits. The modifications include using the STC and CLC commands to activate different logic functions. The three backplane flag and control section PAL's (U1, 2 and 3) have been customized to specifically emulate the HP 13037A PCA.

Addressing a CLC instruction to the PCA sets a 'Command Ready F/F' in addition to clearing the Control F/F. The SFC instruction tests for a 'Controller Busy' condition instead of the clear state of the Flag F/F.

Data transfer between the backplane and the PCA is buffered by a 4 word buffer register. Data between the buffer register and RAM on the PCA is controlled by the V40 DMA. DMA Channel 1 controls data flow from the backplane to RAM while DMA Channel 2 controls data flow from RAM to the backplane.

5.5.1. FLAG/CONTROL SECTION

The flag and control logic is contained in PAL devices U1, U2, and U3. These devices emulate the normal flag and control circuits of the 13037A 21XX I/O card.

The Flag F/F may be directly set by the V40 processor using the Set Flag bit in the Backplane Control Register (see Table 11 - Backplane Control Register Bit Assignments).The Flag remains set as long as the bit is set to a *1*. When setting the Flag F/F, the bit in the Backplane Control Register must be cleared **immediately**! If the register bit is still set when the 21XX executes a CLF instruction, the Flag F/F is not cleared and remains in the SET state. If the 21XX program is in the common `SFS SC, JMP *-1` loop followed by an `OTA SC,C` instruction, there may be less than one 21XX cycle time for the V40 to get the BCR Set Flag bit cleared. Likewise, the Clear Flag bit is used to clear the Flag F/F and will hold the Flag F/F clear as long as it is set. The Busy Status is set by outputting a 0 to the Busy bit. Setting the Busy bit to a *1* will reset the Busy status (a 21XX SFC instruction skips). This is a static bit and the current state must be maintained whenever other bits in the BCR are manipulated.

The Control F/F is primarily managed by the backplane and may only be set by executing a 21XX STC instruction. The Clear Control bit in the Backplane Control Register may be used to reset the Control F/F. The CLC signal from the backplane sets the Command F/F and the BCR Clear Command bit is used to reset the Command F/F.

PAL U3 contains the CONTROL logic for the emulator. For use as an HP 13037A emulator the logic in U3 only responds to the backplane when the LSCL and LSCM signals are asserted indicating an I/O Select Code detection for the PCA Slot. The Upper Select Code Control F/F in U3 serves as the Command F/F and is set to the True state on receipt of the CLC signal from the backplane.

PALs U1 and U2 implement the FLAG and IRQ logic for the emulator. They implement the flag, flag buffer and interrupt request latches. The Flag logic in U1 provides the normal data handshake F/F. This F/F state is tested by the Skip Flag Set (SFS) instruction only. The FLAG F/F located in U2 is the Controller Busy State indicator and is tested by the Skip Flag Clear (SFC) instruction. Either F/F may be set or cleared by the V40 processor.

The backplane DMA service request signal (SRQ) is generated by PAL U28 based on the state of the buffer control logic PAL's for the data input and the data output sections.

5.5.2. INPUT BUFFER SECTION

Data to the Emulator from the 21XX computer is buffered by a 4 word addressable register (U19, U22, U23 and U24). This register allows multiple 21XX OUTPUT instructions to be executed without the V40 missing any data. As data is written into the register, the WRITE buffer *input address* counter (U18A) is incremented. This counter may be read by the V40 to determine the number of words sent to the register. The V40 may then read the contents of the addressable register as needed. Since the V40 external data bus is only 8 bits wide, the data from the register must be read 8 bits (1 byte) at a time. Two separate V40 I/O addresses are used to read the LS and MS bytes. The V40 processor must read both bytes each time to

retain data integrity. The WRITE buffer *output address* counter (U18B) is updated each time the MSB is read. This counter may also be read by the V40 to determine which word is to be read from the buffer.

5.5.3. OUTPUT BUFFER SECTION

Data from the Emulator to the 21XX I/O backplane is stored in a 4 word addressable buffer register (U20, U21, U25 and U26). Because the V40 data bus is only one byte wide, two unique V40 I/O addresses are used to transfer the lower byte and upper byte to the output buffer. The READ buffer *input address* counter (U27A) maintains the current word count in the register and is updated each time a new byte is output by the V40 to the MSB I/O address.

When the 21XX backplane reads the data from the output buffer register, the READ buffer *output address* counter (U27B) is incremented. Again, this counter may be read by the V40 to determine the number of words read by the backplane.

5.5.4. INPUT DMA CONTROL SECTION

PAL's U30 and U35A implement the logic necessary for DMA transfer of data from the 21XX backplane to the Emulator RAM memory. U30 implements a state machine to control sequencing of data read from the WRITE buffer registers. U35A monitors the state of the WRITE buffer input address and output address registers and detects the Empty, 'Full-1', and Full states.

5.5.5. OUTPUT DMA CONTROL SECTION

PAL's U35B andU37 implement the Emulator to Backplane READ buffer control logic and operate similar to the Input section.

5.5.6. SRQ CONTROL

PAL U28 combines the SRQ request signals from the emulator input and output sections to generate the DMA Service Request Signal to the 21XX DMA controller (DCPC). U28 also latches the End of Data Transfer (EDT) signal indicating completion of the HP21XX DMA transfer

5.6. EMULATOR FIRMWARE OPERATION

The following sections describe the program operation of the EMULATOR as the HP13037A replacement.

The SyQuest Technology SQ 3270S Removable Cartridge Drive uses a RLL 2,7 magnetic recording format and has a multi-zone capacity of 256 Mbytes. Multi-zone means the drive does not have a consistent number of sectors per track over the entire radius of the cartridge. Since the SCSI interface addresses the 512 byte sectors using Block numbers, the track layout is essentially invisible to the user. A comparison of the different drive's specifications follows.

The drives referred to in this document have the following characteristics:

Drive	HP 7906	HP 7920	HP 7925	SQ 3270
Heads	2+2	5	9	2
Cylinders	410	823	823	N/A
Sectors/Surface	48	48	64	60 to 100
BYTES/Sector	256	256	256	512
Total Size (Mbytes)	10.1+10.1	50.6	121.4	256
Max. Seek Time (ms)	45	45	48.5	30
Average Seek Time (ms)	25	25	27	13.5
Rotation Rate (rpm)	3600	3600	2700	3600
Rotation time (ms)	16.6	16.6	22.2	16.6
Average Access Time (ms)	33.3	33.3	38.1	38.4
Max Data Transfer Rate	973 Kb/sec	973 Kb/sec	973 Kb/sec	> 1.4 Mb/sec

A means to support the protected track lockout feature of the HP drives is provided. As the SCSI cartridge has capacity for more than one HP unit in all cases, a protected track map table is maintained on the cartridge for each individual platter in an area not used for normal data storage. This map is read from the disk during initialization and is updated as necessary whenever an Initialize command is executed. Sparing and alternate track management is a feature internal to the SCSI drive and is invisible to the operating software, therefore, HP 79XX operations related to Spare tracks are not supported.

The 7906 drive is emulated as up to eight (8) 7906 platters residing on a single SQ 3270 cartridge. Each SQ 3270 cartridge holds a single 10.1 Mbyte *fixed* platter and up to seven 10.1 Mbyte *removable* platters. An external control panel is provided to select which one of the seven removable platters on the cartridge is actually accessed as the 7906 removable platter seen by the 21XX backplane at any single point in time. The 7906 platter selected by the switch controls the data access to heads zero and one of the 7906. The sixteen logical tracks for all eight platters of one 7906 cylinder are mapped into 384 consecutive SCSI blocks. This mapping reduces the amount of SCSI drive head movement necessary to move between the two fixed heads and the current two removable heads set by the Control Panel digit switches. Track mapping for the 7920 and 7925 drives is linear for each pack since only one pack can be active at any point in time.

However, because all eight 7906 platters are physically contained within the single SQ3270 cartridge, a way to move data from one SQ3270 cartridge to another is required. To support this requirement, three scenarios are provided. The first and least complex is to use standard external mass storage peripherals already on the HP system such as 9 track Magnetic Tape, Cartridge Tape, Paper Tape, or any other RTE supported mass storage peripheral (that does not require the 13087 MAC controller interface connected to the SCSI drive), but including a second MAC controller interface configured as a separate RTE EQT. The

other two methods both require installation of another SQ 3270 drive attached to the 91060 interface as a second SCSI device.

In order to support RTE systems configured with a single 7906 drive, it is possible to select the platters on a second SQ3270 drive as incremental additions to those already existing on the first cartridge. In this instance, the user selects the current removable drive from 15 possible options instead of the original 7 on the primary drive. The 7906 platter on the second drive cartridge accessed by switch setting 10 appears as the fixed platter when the cartridge is installed in the primary drive of either HP Unit. The other platters on the auxiliary cartridge are referenced as platters 11 through 17, but appear as platters 1 through 7 if the cartridge is installed in a primary drive. This configuration still permits disk copies only between the primary drive's platter 0 (7906 heads 2 and 3) and whichever second platter is assigned as the removable platter regardless of whether the active platter is physically located on the primary or the secondary drive. However, storing data on the secondary drive allows it to be removed from the system independent of the fixed platter.

NOTE

This method does not allow installing an RTE system configured for the fixed platter on platter 10 using SWTCH! Although platter 10 becomes platter 0 if installed in the primary drive, it appears as the removable platter on the primary drive to SWTCH.

The final method requires the RTE system to be generated with two 7906 drive units designated Unit 0 and Unit 1. In this configuration, the user has access to either physical drive so four platters are simultaneously accessible. Cross copying is possible from either the fixed or removable platter on one HP Unit to either platter on the other. The fixed platter on each cartridge is referenced as platter 0. The external switches allow assignment of platters 1 through 7 on each cartridge as the current removable for that cartridge.

5.6.1. CONTROLLER INTERFACE

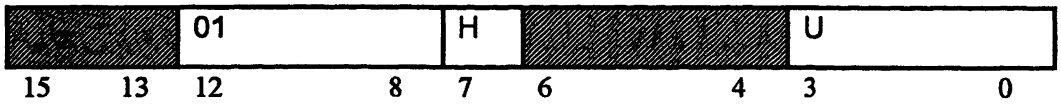
Table 9 - Controller Commands contains the entire list of 13037 command codes. Commands with limited or no support on the 91060 Emulator Interface are indicated.

The following paragraphs describe the commands as implemented for the 91060 SCSI interface card.

5.6.2. CONTROL COMMANDS

Control commands start operations not involving a transfer of data sectors between the interface and computer. Instead these commands are used to establish certain known conditions within the interface or disc drive. The hold bit though included in the commands, has no action within the 91060 interface.

5.6.2.1.RECALIBRATE



H = Hold bit (Not Supported) U = Unit number

The RECALIBRATE (SEEK HOME) command provides the operating system with a means of restoring the disc drive's heads over a known cylinder (always 0) after that drive is suspected of having lost track of its exact position. To perform this command, only the command word is necessary. The word contains only the opcode, the hold bit, and unit number. If the addressed unit is available and ready, the interface issues a

RECALIBRATE command. The disc drive positions its heads over logical cylinder 0 and clears its *current cylinder address* and *current head/sector address* registers.

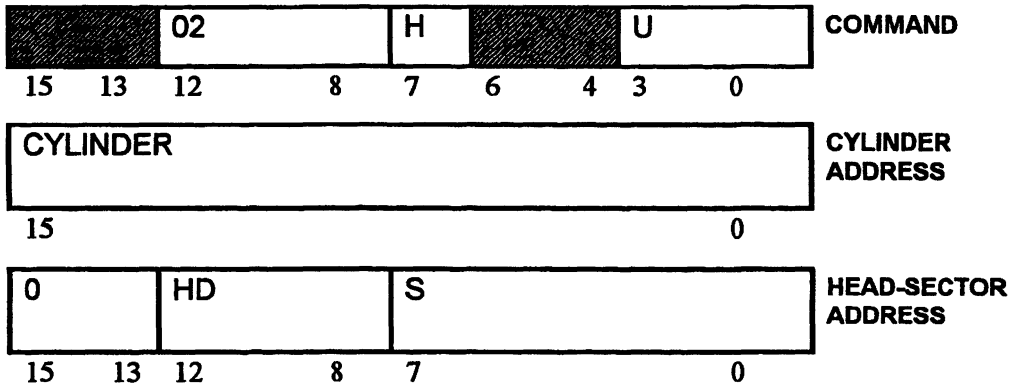
TABLE 9 - CONTROLLER COMMANDS

CODE	COMMAND AND GROUP			
(OCTAL)	CONTROL	SENSE	READ	WRITE
00			Cold Load Read	
01	Recalibrate			
02	Seek			
03		Request Status		
04		Request Sector Address		
05			Read	
06			‡ Read Full Sector	
07			Verify	
10				Write
11				§ Write Full Sector
12	Clear			
13				Initialize
14	Address Record			
15		§ Request Syndrome		
16			‡ Read with Offset	
17	‡ Set File Mask			
22			‡ Read without Verify	
23		Load TIO Register		
24		Request Disc Address		
25	End			
26	Wakeup			

‡ Command Partially supported (returns a satisfactory status or legal response as applicable)
§ Command NOT supported (use always returns Illegal Opcode status)

If a unit number greater than 10 (octal) is requested, the CPU will be interrupted with a "unit unavailable" error. If the drive unit is available, but will not respond and the interface Control FF is set, the interface Flag FF is set after the appropriate Status 2 word is generated. While technically not required with the SCSI drives, the command still performs the same task.

5.6.2.2.SEEK



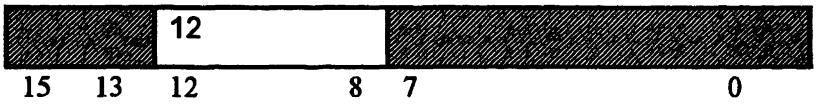
H = Hold bit (Not Supported) HD = Head address
U = Unit number S = Sector address

The SEEK command causes positioning of the disc drive's heads over the desired logical cylinder; at the same time the interface will store the transmitted cylinder, head, and sector address in its internal registers. This instruction is initiated by issuing the command word followed by two additional words in the order shown. The first contains the cylinder address and the second contains the head and sector address. The interface requests each of these words by setting the interface Flag FF. The interface processor then converts them to the SCSI block number with the sector address of 0. The SCSI block number is transmitted to the disc drive using a SCSI **Read** command for a full track based on the drive type. Once the read is initiated, Status Request Commands may be processed which will inform the 21mx the drive is still busy. When the read is completed, Attention Status is returned. If no command is pending, the CPU generated Set Control FF is checked to see if a subsequent interrupt is allowed. If the Control FF is set, the program sets the Flag FF. The interface waits for the next command. If the Control FF is not set, the interface will wait until another command transfer occurs or the Control FF is set, after which the Flag FF will be set.

If a unit number greater than 10 (octal) is requested, after the Control FF is set, the Flag FF will be set with a "unit unavailable" error in Status-1. No data transfer is initiated. Unit numbers with no drive attached return a Normal Completion response with Status 2 set to Drive Not Ready. If the drive unit is available but not ready, the address words are stored in interface memory, the status words are updated to indicate the not ready condition and when the Control FF is set, the interface sets the Flag FF.

Note: the target head, sector, and cylinder address are retained in the interface memory for future data operations, but are overwritten by a subsequent ADDRESS RECORD or SEEK command.

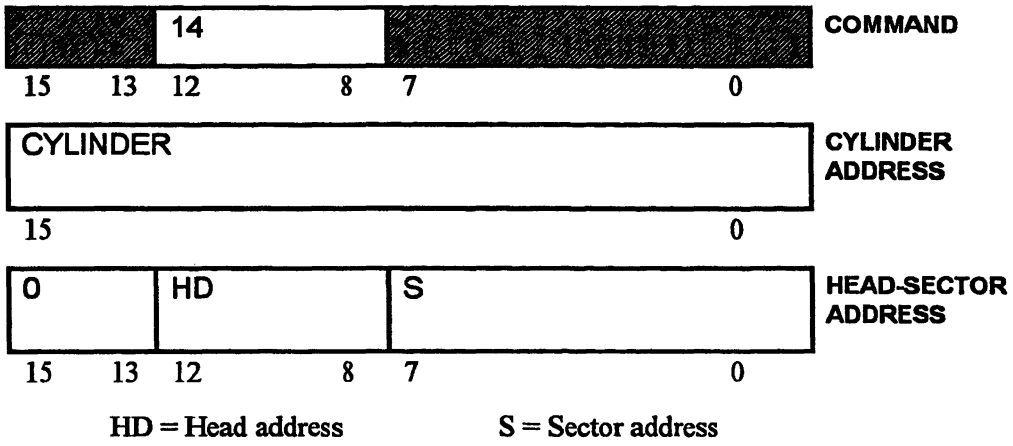
5.6.2.3.CLEAR



Upon receipt, the interface issues a SCSI RESET and a REQUEST SENSE command to each active drive. Status of each drive is updated in interface memory. The interface sets the Flag FF and waits for the next command. A unit number is not required.

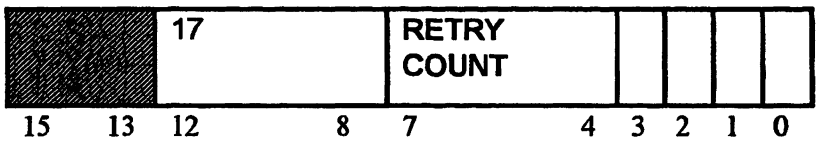
Note: the software clear command differs from the "hard clear". The latter unconditionally resets the interface to its power-on state (i.e., all CPU/drive mapping is reset, current command processing is lost, etc.).

5.6.2.4.ADDRESS RECORD



In the HP 13037 this command is used to set a logical address in the controller without transmitting it to the disc drive. The BKR 91060 processes this command as a seek if the cylinder/head/sector value is different from that of the most recent seek address for the drive unit number. The command is treated as a NOP if the specified address is identical to the most recent seek address. The issuance of the command word by the CPU is followed by two words in the order shown. The first contains the cylinder address and the second contains the head and sector address. The interface requests each of these words by setting the Flag FF after the first and second words are received. After the third word is received, the interface performs a seek as previously stated or just sets the Flag FF and waits for a new command.

5.6.2.5.SET FILE MASK



This command is implemented in the 91060 except for the Retry Count (used only on the HP 3000) and sparing. The Sparing bit is accepted, but ignored. Sparing is automatically implemented by the SCSI drive. Retry count is a drive controlled function and is set to 4.

In the HP 13037, bit 0, when set, allows the controller to automatically seek to the next higher or lower cylinder address (depending on bit 3) when a data operation continues through the end of the current logical cylinder. The new track is subjected to disc address and track status verification before any further operation is performed. When bit 0 is clear, the option is prohibited, and any data operation which exceeds the end of the current cylinder is aborted with an end-of-cylinder error status. In the 91060, this feature is supported for next higher cylinder only.

Bit 1, when set, indicates that the controller is operating in the cylinder mode. In this mode, the first head address is 0 (the top-most head) and head switching occurs automatically following the last data sector of each track. The head address increases incrementally from 0 to the last head address of the particular disc drive. As each new head is switched in, the verification described in the previous paragraph is performed. The last data sector of the last head address of the current track address is the end of the logical cylinder.

In the HP 13037, when bit 1 is clear, the controller is operating in the surface mode, where the head address never changes. The last sector of the current track address is the end of cylinder. If bit 0 is set (incremental/decremental seek allowed), a data operation which exceeds the end of the cylinder will continue at the next higher/lower cylinder address (subject to address and track status verification). In the 91060, this feature is supported for incremental head operations only.

In the HP 13037, when bit 2 is set, the controller is allowed to automatically seek to previously initialized spare tracks when a defective track (that is, one which has been initialized defective) is encountered. (The entire spare track algorithm will be described later.) If bit 2 is clear, the automatic sparing will not occur and a defective track error status will be reported to the interface. The 91060 always operates as if this bit were set, whether or not it is 1 or 0.

In the HP 13037, Bit 3 operates in conjunction with bit 0 and determines whether an automatic end-of cylinder seek will be to the next higher or lower track address. If bit 3 is 0, the next higher track is selected; if it is 1, the next lower track is selected. Note: Due to an anomaly in the 13037 microcode, setting bit 3 to a 1 causes an automatic seek to the next higher cylinder after the last sector of the last head is transferred **without regard to the state of bit 0**.

In the HP 13037, Bits 4 through 7 indicate how many retries are allowed, but is not used in 21XX computers. In the BKR 91060, the number is ignored as the number of retries is a disk rather than an interface function.

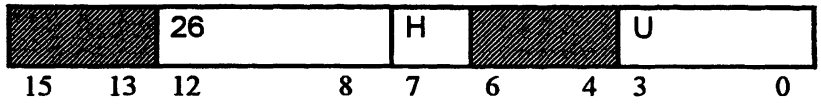
The mask sets the mode of operation for the controller. The controller transfers bits 0 - 3 into its "mask" register which is used to control the action taken while transferring data. At power up, the 91060 mask is set to 0 (no-automatic-seek, and surface mode).

Because the file mask affects both sparing operations and data transfers that require crossing over the last sector of a particular logical 79xx cylinder, the condition of the file mask must always be known by the operating system. A time-out error will reset the 91060 file mask to the "no automatic seek, surface mode" state.

5.6.2.6.END

In the 13037, this command is used to avoid a time-out if no other command is expected to be outputted from an interface and the controller is waiting for a command from that interface. When the controller accepts this command from an interface, no action is taken except to disable time-outs. This command should follow any string of commands when they have been completed. In the 91060, this command immediately allows SCSI Drive Status requests. This command **does not set the Flag FF** upon completion.

5.6.2.7.WAKEUP



H = Hold bit (Not Supported) U = Unit number

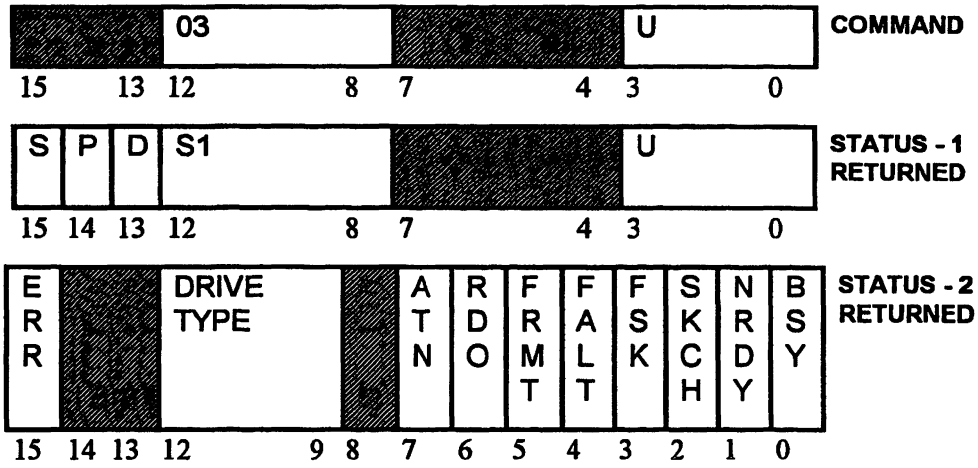
This command checks if the specified unit is available. If not, no action is taken. If the unit is available, the status register is set to indicate "unit available" and the interface Flag FF is set.

It is suggested that if the WAKEUP command is used, a REQUEST STATUS command should follow to determine the condition of the accessed drive prior to its use.

5.6.3. SENSE COMMANDS

Sense commands are included as a means of providing feedback to the operating system as to the condition of the interface, disc drive, or various operations. Included in this group are diagnostic and data recovery commands that expand the versatility of the 91060 interface and enhance the reliability of data transfers. Availability of the information is accompanied by setting the Flag FF.

5.6.3.1.REQUEST STATUS


03
U
COMMAND
15 13 12 8 7 4 3 0
S P D S1 U
STATUS - 1 RETURNED
15 14 13 12 8 7 4 3 0
ERR DRIVE TYPE ATN RDO FRMT FALT FSK SKCH NRDY BSY
STATUS - 2 RETURNED
15 14 13 12 9 8 7 6 5 4 3 2 1 0

U Unit number to which status on last operation applies; if S1 is 37 (drive attention), U is number of interrupting drive. If no unit number is appropriate, U will be zero.

S1 Encoded termination status (octal).

After receipt of the command, the two status words can be read by two consecutive inputs to the CPU interface. The first (Status-1) contains information relating to the last operation performed, and the second (Status-2) contains information pertaining to the disc drive addressed in the command word. The *First Status* bit (3) in Status-2 is cleared by this command after it has been read the first time since power up. Note: the unit field of the command word sets the drive the returned Status-2 word describes, while the unit field of the Status-1 word relates to the drive associated with the last operation performed.

S Spare track (Not Supported)

P Protected track - Supported

D Defective track (Not Supported)

The various encoded termination status values in the S1 field are explained below. The 13037 values listed as not supported can never occur on the 91060.

00 NORMAL COMPLETION. This status is transmitted in one of two situations:

a. When the previous command has been fully executed without error.

b. At completion of a REQUEST STATUS command whenever the command immediately follows another REQUEST STATUS command or when it is the first command issued after the interface has been reset. For the latter case, the U field will be zero.

01 ILLEGAL OPCODE. A command word has been received by the interface of which bits 12-8 contain a command code which is not one of interface's command set.

02 UNIT AVAILABLE. Interface transmits this status after interface has put out a WAKEUP command for a specific drive and that drive has become available.

07 CYLINDER COMPARE ERROR. Not supported.

10 UNCORRECTABLE DATA ERROR. This status is generated by the interface immediately following a data transfer (or VERIFY) command if an error is returned by the drive.

11 HEAD-SECTOR COMPARE ERROR. Not supported.

12 I/O PROGRAM ERROR. Not supported.

14 END OF CYLINDER. A multiple-sector data transfer must continue beyond end-of-logical-cylinder, but file mask will not allow interface to automatically seek to next logical cylinder and continue.

16 OVERRUN. Not supported.

17 POSSIBLY CORRECTABLE DATA ERROR. Not Supported.

20 ILLEGAL ACCESS TO SPARE TRACK. Not Supported

21 DEFECTIVE TRACK. Not Supported

22 ACCESS NOT READY DURING DATA OPERATION. Not Supported

23 STATUS-2 ERROR. The interface is unable to complete a command due to some condition in disc drive. The Status-2 word may be examined for reason. Examples of Status-2 Errors are:

a. An Initialize command is issued, but Format switch is off or the WRITE PROTECT switch is set ON.

b. A command is issued to a drive which is Not Ready (heads unloaded) or for which a Drive Fault has occurred.

26 ATTEMPT TO WRITE ON PROTECTED TRACK. During verification of track status of the first sector to be written to using a Write command, the P bit is found to be set and the Interface Format switch is OFF.

27 UNIT UNAVAILABLE. This status is returned whenever the U field of the command word is greater than 12 (octal).

37 DRIVE ATTENTION. Interface sets the Flag FF to the CPU whenever:

a. Drive is requesting attention and,

b. Control FF is set, thereby allowing attention interrupts.

Briefly, conditions causing a drive to request attention are any one of the following:

a. Seek completion.

b. Drive becomes ready (heads load).

c. Drive becomes not ready (heads unload).

d. Seek check.

e. Drive Fault.

Status-2 Unit status

Bit

0* Drive busy

1* Drive not ready

2* Seek check

3 First status

4* Fault

5 Format (this reports the position of the Format Switch on the Drive Panel)

6 Protected (drive cannot write) Status of Drive Panel Upper/Lower Protect Switch

7 Attention

8 (Reserved)

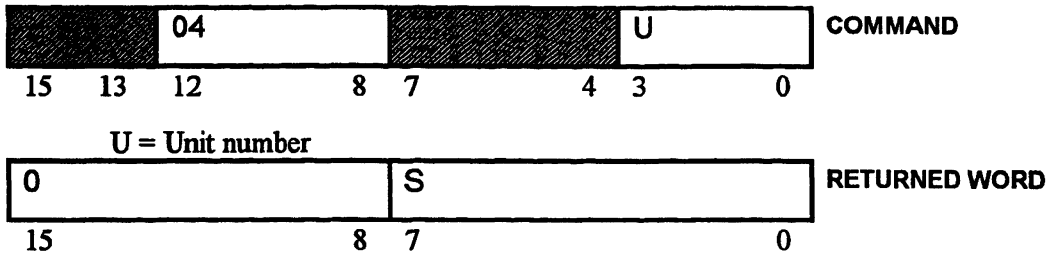
9-12 Encoded drive type (used by interface to determine last available head and sector) as described below.

15 Status-2 error (true whenever any bit marked * is true)

DRIVE TYPES:

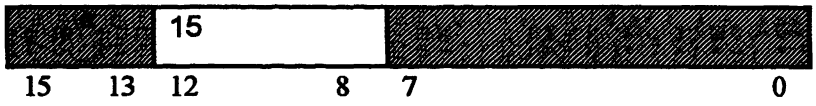
0 7906 (4 heads, 48 sectors)
1 7920 (5 heads, 48 sectors)
2 7905 (3 heads, 48 sectors) Not Supported
3 7925 (9 heads, 64 sectors)

5.6.3.2.REQUEST SECTOR ADDRESS



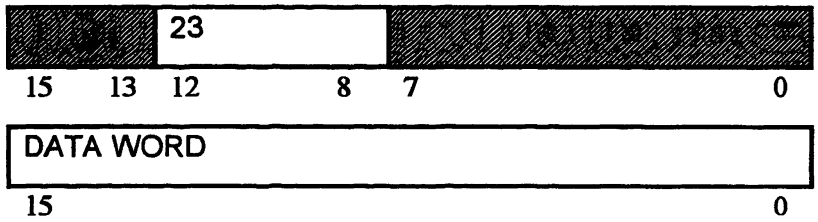
In the HP 13037, after receipt of this command, the controller returns the logical address of the sector currently passing under the heads of the specified unit. At completion, the controller waits for the next command (or a time-out). In the BKR 91060, the last requested sector number minus one is always returned indicating the requested sector is about to be read as it is already in the Interface memory. Subsequent contiguous Request Sector Commands return sequentially higher sector addresses in case the program is looking for changes due to *rotation*.

5.6.3.3. REQUEST SYNDROME



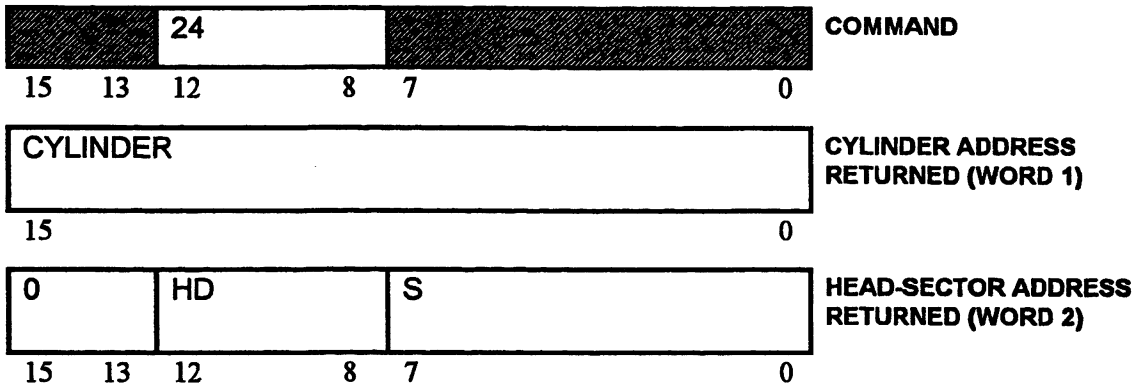
This command is not supported. (Used for *possibly correctable error* which cannot occur on the BKR 91060.)

5.6.3.4. LOAD T10 REGISTER



In the 13037 it is included as a diagnostic tool. The LOAD TIO REGISTER command allows the CPU to accept information and write it into the controller's TIO register much as the Status-1 word is automatically written into that register after every controller operation. The controller requests a data word by issuing STDFL. This data word is then written into the TIO (status) register on the interface by a Write Interface Status Register (WRTIO) order. The controller then transmits Request Service (RQSRV) to the interface and waits for a new command (or time-out). This command is only used on the HP 3000 Interface. It is not supported by the BKR 91060A.

5.6.3.5.REQUEST DISC ADDRESS



HD = Head address S = Sector address

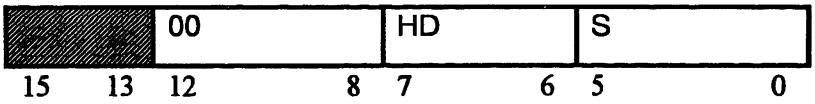
The interface returns two words in the order and format of the address words passed in a SEEK command. The command may be used at any time, but is most useful following a multiple-sector I/O or VERIFY command which aborted with an error. This command allows the operating system to determine where the abort occurred.

The returned address is that of the most recently addressed disc unit. This will be the address of the sector triggering an error if a data error has occurred or the address of the next logical sector following the last transfer if no data error occurred.

5.6.4. READ COMMANDS

Read commands transfer information from a disc drive to the computer. Because the interface always expects to transfer complete sectors (128 words) to the CPU, any error indications will occur at the end of a sector. Note: ETD can be asserted by the CPU at any time during a sector indicating only part of a sector is to be transferred. The interface will terminate the backplane transfer. All transfers result in the Flag FF being set on the CPU backplane. The operating system must inspect status on apparent completion to check the state of the preceding data transfer.

5.6.4.1. COLD LOAD READ

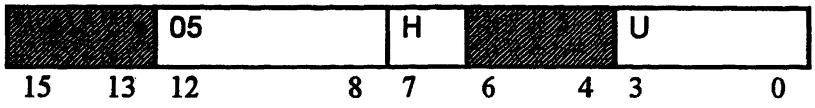


HD = Head address S = Sector address

After issuing a **READ** to unit 0 for a block starting at the equivalent of cylinder 0 and the head and sector specified in the command word. The interface reads all blocks from sector 0 to the end of logical cylinder 0 for the head specified.

At the conclusion of the read, the interface begins to transfer 128 words per sector beginning with the sector specified until the CPU sets the EDT signal or the entire track has been transferred. The Flag FF is set at the end of the transfer with the appropriate status available to indicate if any errors that were detected during either the read or transfer regardless of EDT status.

5.6.4.2. READ



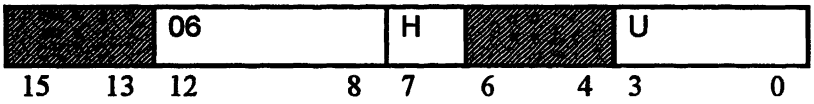
H = Hold bit U = Unit number

Upon receipt of the READ command, the interface begins transferring the 256 bytes of the first block already in memory using the interface's backplane transmit DMA channel.

At the conclusion of each 256 byte data block, the interface continues to setup and transfer consecutive 256 byte blocks until the End Data Transfer (EDT) signal on the backplane is detected. The last sector does not have to be completely transferred. If end of track occurs before EDT and the file mask is set for auto-seek, the next track is read from the disk and the data transfer to the backplane continues as soon as the track data is in memory.

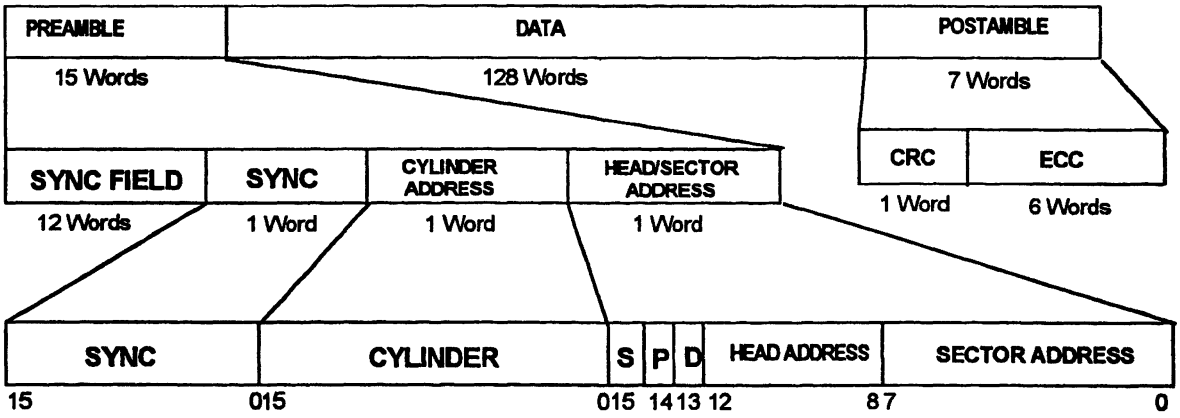
On completion, the Flag FF is set and the Status-1 word made available to be read. The CPU program is expected to read the status word to determine if the transfer was satisfactory or not and take appropriate action.

5.6.4.3.READ FULL SECTOR

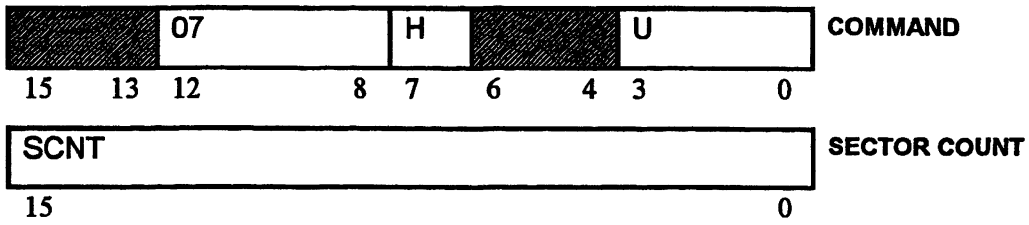


H = Hold bit U = Unit number

The structure of a 79xx disk drive sector is presented below. A Read Full Sector command returns an interface generated 138 word data block beginning with the last three words of the Preamble, then the 128 data words followed by seven zero words. The three preamble words contain the current cylinder, head and sector address being accessed. The SYNC word always contain 10376_8 indicating a valid ECC field. While the 128 words of data are correct for the specified sector, the CRC and six ECC words included at the end of the transfer are all zeros and, therefore, are NOT valid. Read Full Sector is used by some programs to verify the current programmed disk address. Only one sector is transferred for each Read Full Sector command.



5.6.4.4.VERIFY



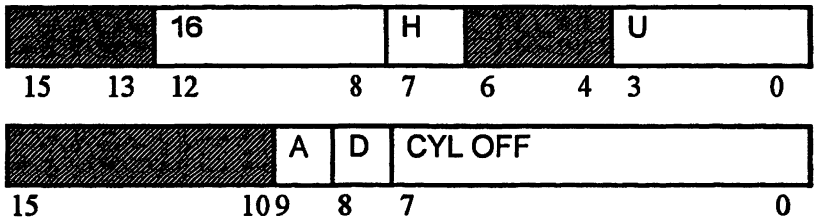
H= Hold bit U = Unit number
SCNT = Sector count

The interface first checks that the specified unit is available and if not, sets the Flag FF with the appropriate status words available. The following description assumes the unit is available.

After acceptance of the command word, the interface requests the sector count (SCNT) by setting the Flag FF to the backplane. Starting with the currently addressed sector, the interface issues a SCSI VERIFY command to the selected disk unit with a verification length of SCNT divided by 2. At completion or on error, the SCSI status is tested, Status-1 is made available for reading at the 21XX backplane and the Flag FF set. The SCNT designates how many sectors are to be verified. If SCNT is zero, the interpretation is 65,536 (decimal) sectors which translates to 32,768 SCSI Blocks.

The SCSI block number the interface sends to the disk drive is the determined by (1) the sector last addressed by a SEEK command; (2) the sector last addressed by an ADDRESS RECORD command; or (3) the sector following the sector last transferred, whichever occurred most recently. If either the sector count or starting sector number results in an odd number of 256 byte sectors to be verified, the verify will begin at either the previous even numbered sector or be extended to the end of the last sector normally verified.

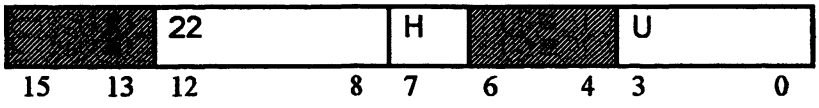
5.6.4.5.READ WITH OFFSET



H = Hold bit A = Advance clock*
U = Unit number D = Delay clock*
CYL OFF = Cylinder offset magnitude

Offset word is ignored. Command is executed as a normal READ command.

5.6.4.6.READ WITHOUT VERIFY



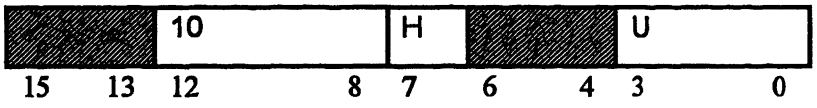
H = Hold bit U = Unit number

Command is executed as a normal READ command.

5.6.5. WRITE COMMANDS

Write commands transfer information from the 21XX computer to the interface for subsequent writing onto the disc. 128 words per sector are transferred until the CPU sets EDT or until the interface is unable to continue the transfer due to a drive error, or condition set in the file mask. Existing data from the track being written is always present in memory before data is transferred from the backplane. Write data is transferred into a buffer until EDT or end of track occurs. This allows the maximum amount of data to be transferred to the disk with each SCSI write operation. Because the interface always processes complete sectors, normal completion or any errors that occur will be reported at the end of the last sector. In the event EDT is asserted prior to the end of a sector, the interface writes the last transmitted word into the remainder of the sector data field before it is written to the SCSI drive. If a write command begins writing on an ODD sector number, i.e. half way through a 512 byte SCSI block, the first sector in the block is copied from the read buffer to the write buffer before the new block is written to the disk. Should EDT cause the write to end after only half of the SCSI block is filled, the data from the second half of that SCSI block is transferred from the read buffer to the write buffer prior to writing the block to the disk. The Flag FF will be set after the last block is written to the disk. If the write to the drive is successful, the appropriate blocks in the read buffer are updated with the write buffer contents.

5.6.5.1.WRITE



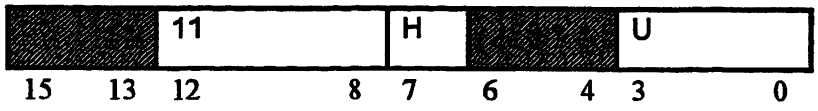
H = Hold bit U = Unit number

On receipt of the command word, the interface checks that the cartridge/platter is not protected because the WRITE PROTECT (READ ONLY) Control Panel switch in the ON position. The following description assumes the unit is available and the WRITE PROTECT switch is in the OFF position. The current cylinder/head address are checked against the track protect bits maintained by the interface. If the track has been protected and the FORMAT switch is in the OFF position, the command is terminated with an ATTEMPT TO WRITE ON PROTECTED TRACK status. If the FORMAT switch is in the ON position, the write proceeds normally regardless of the state of the protect bits.

The interface accepts the data in 128 word blocks from the 21XX backplane until EDT is set or End of Track is reached. The interface begins writing on (1) the SCSI block defined by the sector last addressed by a SEEK command; (2) the SCSI block defined by the sector last addressed by an ADDRESS RECORD command; or (3) the SCSI block defined by the sector following the last sector transferred, whichever occurred most recently.

On all data transfers out of the computer, the interface expects 256 bytes (128 words) of data. If the computer transfers less by setting EDT, the interface repeatedly writes the last transmitted word into the remainder of the sector data field. If the transfer ends on an even numbered sector, the odd numbered sector is filled with data previously read from the block on the disk during the initial read of the track started by the seek command. If end of Track occurs before EDT data transfer from the backplane is stopped. If the File mask is not set for Auto Seek, an End of Cylinder error condition is generated after the current track data is written to the disk. If the file mask is set for Auto Seek, the internal cylinder and head addresses are updated, the next track is read from the disk and data transfer from the backplane resumes continuing the previous process. On completion of the write to the disk, the Flag FF is set at the 21XX backplane.

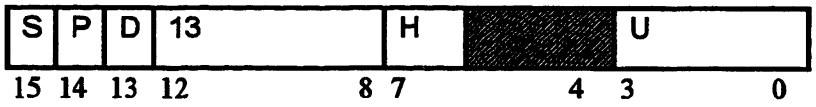
5.6.5.2.WRITE FULL SECTOR



H = Hold bit U = Unit number

Command is Not Supported. Returns Illegal Opcode in Status 1.

5.6.5.3.INITIALIZE



S = Flag track spare (Not Supported)
P = Flag track protected
D = Flag defective (Not Supported)
H = Hold bit (Not Supported)
U = Unit number

This command is similar to a Write command except it is also used to set or clear the protect bit for a track. Only full tracks (cylinder + head address) may be protected. On receipt of an Initialize command word, the interface checks that the pack (platter for 7906) is not protected by the drive WRITE PROTECT (READ ONLY) switch set to the ON position and that the FORMAT switch is set to ON before executing the command. The interface then begins requesting data from the computer and writes 128 data words on the addressed sector. Data transfer continues until the CPU sets the End Data Transfer (EDT) bit. The following description assumes the HP unit is writable.

The interface begins writing on (1) the SCSI block defined by the cylinder, head and sector last addressed by a SEEK command; (2) the SCSI block defined by the cylinder and head last addressed by a SEEK command and the sector last addressed by an ADDRESS RECORD command; or (3) the SCSI block defined by the sector following the last sector transferred, whichever occurred most recently.

On all data transfers out of the 21XX, the interface expects 128 words (256 bytes) of data. If the 21XX transfers less by setting EDT, the interface repeatedly writes the last transmitted word into the remainder of the sector data field. If the transfer ends on an even numbered sector, the odd numbered sector is filled with data previously read from the block during the track read initiated by the seek command. On completion of the write to the disk, the Flag FF is set at the 21XX backplane. Assuming the normal data write to the SCSI drive is successful, the data protect block(s) are updated if a change in protect status for the track occurred. Should more than one track be written, the protect block update is deferred until the final transfer to the drive has successfully taken place.

Bit 14 of the command word is used to flag the track protected. Subsequently, when a data transfer (or VERIFY) operation is attempted on a track so marked, the status of the track last accessed by that operation will appear in bit 14 of STATUS-1 word.

5.7. INTERNAL SOFTWARE OPERATION

5.7.1. TRACK CACHING

To achieve maximum performance, the BKR 91060 makes use of on-board RAM memory to buffer data to and from the SCSI drive. Whenever a SEEK command is issued by the 21XX, the entire track referenced in the command is read into memory. Subsequent reads or writes to data on that track make use of the data

present in RAM as appropriate. Up to eight 7906/20 tracks or six 7925 tracks cached on a least recently used basis. A separate cache is maintained for HP Unit 0 and HP Unit 1. The entire cache for a unit is invalidated whenever a cartridge change is sensed.

5.7.2. 79XX CARTRIDGE DRIVE TYPE

The specific 79XX drive type information which identifies the drive being emulated is stored in the Vendor ID page on each SCSI removable cartridge. It is returned by the drive to the Interface using a SCSI INQUIRY command. The interface sets the appropriate drive type bits in the Status 2 word returned to the 21XX in response to the HP Request Sense command. The interface returns a NOT READY status if the cartridge in the drive has not been properly initialized or if no cartridge is mounted in the drive. HP Request Sense commands addressed to HP Units 2 through 7 always return a Status 1 of NORMAL COMPLETION with the DRIVE NOT READY bit set in Status 2. The drive type is written on the cartridge using a combination of Interface DIP switch and Control Panel switch settings. Refer to the Cartridge Initialization Section for specific details of this procedure.

6. PROGRAM DEVELOPMENT

This section provides information to support the development of software to operate on the 91060A MAC DISK EMULATOR PCA. All software for the PCA may be developed on an IBM PC or compatible computer using standard program development tools. The following development tools are recommended for use in program development.

1. Borland C or C++ Professional Compiler w/
   Turbo Debug and Turbo Assembler (Version 3.0 or later)
2. Paradigm TDREM
3. Paradigm LOCATE
4. Paradigm Debug/RT(not required, but recommended)

These tools allow the programmer to develop software in either 'C' or Assembler under the DOS operating system. The Paradigm TDREM package provides a Borland Turbo Debug compatible kernel for operation on the target system (MAC DISK EMULATOR PCA). Source level debug of programs may then be accomplished using either TurboDebug or Paradigm's Debug/RT. Additional documentation may also be necessary for program development. Copies of the NEC V40 Users Manual and the NCR 53C90A Data Booklet should be available. This section provides programming information specific to the Emulator PCA. Development of Emulator programs requires persons trained in the 'C' language, Intel 808x Assembler programming, HP 21XX Computer assembly language, SCSI-1 Bus operations and 21XX I/O card operation.

These tools are available from:

Borland International
100 Borland Way
Scotts Valley, CA 95067 USA
(408) 438-8400

Paradigm Systems
3301 Country Club Rd, Ste 2214
Endwell, NY 13760 USA
(607) 748-5966

6.1. PROCESSOR MEMORY ALLOCATION

The V40 Processor supports a 1 MBYTE data space. The Emulator PCA provides capability to install up to 256 Kbytes of RAM beginning at 0:0 and up to 256 KBYTES of EPROM ending at F:FFFF. The first 1 Kbyte of RAM is normally reserved for interrupt vectors. Remaining RAM is available to the user. All input and output to the backplane, SCSI Controller, and other devices is accomplished using the I/O bus. No I/O devices are memory mapped.

6.2. PROCESSOR I/O ASSIGNMENTS

The NEC V40 contains a number of on-chip peripheral devices. During the power-up or reset sequences, the programmer must properly initialized any of these devices to be used. The V40 uses

a reserved section of I/O space from FF00 to FFFF for initial setup of the on-chip device addresses and their operation. The following I/O addresses are recommended for use by the on-chip devices.

OPHA-BASE	0x00	On-Chip Peripheral High Address Base
IULA-BASE	0x20	Interrupt Controller Base
TULA-BASE	0x40	Timer/Counter Base
SULA-BASE	0x60	Serial Unit Base
DULA-BASE	0x80	DMA Unit Lower address Base

Additional On-Chip peripheral programming information is contained in the NEC V40 Users Manual.

6.3. SCSI PROGRAMMING

Detailed SCSI programming information is beyond the scope of this document. The programmer should refer to the SCSI-1 Specification and the NCR programming data for detail information the following information provides some general information regarding the specific SCSI interface.

The 91060 Emulator uses an NCR 53C90A Advanced SCSI Controller (ASC) to provide a higher level SCSI programming. The device reduces protocol overhead by performing the common SCSI algorithms, or sequences, in response to a single C90A command. The ASC command set allows the common SCSI sequences to execute at hardware speed without host CPU intervention. The on-chip FIFO may be accessed simultaneously by the SCSI bus and the host processor or host DMA controller. All command, data, status, and message bytes pass through the FIFO to or from the SCSI bus. Most ASC commands have two versions: DMA and non-DMA. When DMA instructions are used, data passes between memory and the SCSI bus with the FIFO acting as a temporary storage if the DMA channel is shut down by a higher priority event.

The FIFO also helps enhance execution during non-DMA transfers. For example, the host processor will load a message byte and the Command Descriptor Block (CDB) into the FIFO, issue a selection command and wait for the INT bit to come true in the Status Register. The ASC waits for bus-free, arbitrates for the bus until it acquires it, send the message byte followed by the CDB and sets the Interrupt bit.

For additional details on the operation of the 53C90A, refer to the NCR SCSI Products' 53C90A/53C90B Specification Document *SCSIP-53C90A/B.* This document is available from:

NCR Microelectronics Products Division
1635 Aeroplaza Drive
Colorado Springs, CO 80916 USA
(719) 596-5611

NCR also maintains a public BBS from which 53C90 example programs can be downloaded. The BBS telephone number is (719) 569-1649.

In addition, SCSI programming requires an in-depth knowledge of the SCSI drive used in the emulator. The Technical Reference Manual for the drive is a necessity. The MAC Emulator uses SyQuest SQ3270S drives. The manual for this drive is Part Number 103018-004 and is available from:

SyQuest Technology
47071 Bayside Parkway
Fremont, CA 94538-6517 USA
(510) 226-4000.

Access to the X3.131-1986 SCSI-1 standard document is helpful. The document is available from:

American National Standards Institute (ANSI)
1430 Broadway
New York, NY 10018 USA

NCR also maintains a SCSI BBS (different from the Microelectronics Products BBS listed above). This BBS is devoted to the SCSI Standard. Parts of the SCSI Standard can be downloaded from this BBS. The telephone number of the SCSI BBS is (719) 574-0424.

A good SCSI bus monitor is a definite asset when developing programs to control SCSI devices. SCSI Transactions occur at bus speed and devices will often time out if single stepping is attempted.

6.4. BACKPLANE I/O PROGRAMMING

Program communication with the 21XX I/O backplane is accomplished through input and output buffer registers on the Emulator PCA. Data output from the 21XX is buffered by a 4 word Buffer Register. Data sent to the 21XX is also buffered in a separate 4 word addressable buffer.

The PCA is designed to respond to only the Lower Select Code (LSC). The Higher Select Code (HSC) is not used. To provide the necessary logic to emulate the MAC controller interface, the HSC logic has been replaced with logic necessary for the Emulator Command Ready F/F and Busy F/F.

Table 10 - Control and Status I/O Addresses, in APPENDIX A, provides I/O address information for registers used to control Backplane transfers and should be referred to during the following description of Backplane programming. Four 8 bit registers are used to provide control and status information on the backplane. These registers are the Backplane Control Register (BPCR), the Backplane Status Register (BPSR), the Buffer Control Register (BCR) and the Buffer Status Register (BSR).

The BPCR is an **output only** register and is used to control the PCA Backplane handshake logic. Bits 0 and 1 control clearing and setting of the Flag F/F. To clear or set the F/F the respective bit should be set to a logic '1' and then returned to a logic '0'. Since the registers are held set or clear while these bits are asserted, they should be deasserted quickly. Bits 4 and 5 clear the Control F/F and the Command F/F respectively. Bit 7 controls the Busy F/F and should be left in the logic '1' state for the Controller **NOT BUSY** condition. The state of the Busy bit must be maintained while changing the other bits.

The Backplane Status Register (BPSR) provides current information on the PCA Backplane state. Bits 0 and 1 indicate the state of the READ Buffer (Output from the Emulator to the Backplane). Bits 2 and 3 indicate the state of the WRITE buffer (Input from the Backplane to the Emulator). Bits 4,5,and 6 indicate the state of the Command F/F, Control F/F and Flag F/F respectfully. Bit 7 indicates the state of the End Data Transfer F/F and is set by the 21XX when the DCPC completes a DMA data transfer.

The Buffer Control Register (BCR) is used to enable the Backplane/V40 DMA logic and to reset the READ and WRITE buffer registers. Bit 0 is set to enable WRITE DMA (DMA data transfer from the Backplane). Bit 1 is set to enable READ DMA (DMA data transfer to the Backplane). Bits 5 and 6 are used to reset the WRITE and READ buffer address registers. To reset a buffer register address, the proper bit should be set and then cleared. Bit 7 is the EDT Status F/F reset and clears the EDT F/F after the processor has detected the EDT state.

The Buffer Status Register (BSR) provides current information on the state of the READ and WRITE buffer registers. Each buffer register has 4 locations into which data is saved during backplane transfers. Each register has an input address and an output address. Thus Bits 0 and 1 represent the input address of the WRITE buffer, and indicate the number of words written to the Emulator by the 21XX. Bits 2 and 3 represent the number of words read by the Emulator from the WRITE buffer and when compared with Bits 0 and 1 will indicate the number of words in the buffer which have not been read. Bits 4 through 7 are used for the READ buffer in a similar manner.

6.5. PROGRAM DEVELOPMENT

Development of programs for the Emulator may be accomplished under DOS on an IBM PC or compatible computer. Either Assembler or 'C' may be used as a source language. The most effective means of program development will depend upon the user and user skills. The use of Paradigm's LOCATE, TDREM, and Borland's Turbo-C with Turbo Debug are effective in program development. Paradigm's Debug/RT provides a more capable remote debug environment.

As the Emulator does not have hardware for disks, keyboard, CRT, or other devices that DOS may normally support, care must be used when using high level languages. Library routines which call any device not supported by the Emulator may cause unpredictable results. The Paradigm LOCATE package provides facilities to strip compiler libraries of offending modules. The user may choose to provide dummy modules or leave the modules undefined. Any calls to undefined modules will then be evident during the linking process and steps can be taken to prevent calls to the offending functions. The Borland Turbo Debug and Paradigm TDREM packages can be used to accomplish program debug. Once debug is completed, the LOCATE package is used to create a 'ROMMABLE' version of the code. This code is the programmed into PROM. Paradigm also provides memory management functions to allow use of standard memory allocation functions (malloc(), etc.).

6.6. PROGRAM DEBUG

The Emulator PCA includes a serial port specifically for connection to a PC compatible computer for program debug. As indicated above, the Borland Turbo Debug and Paradigm TDREM provide effective debugging tools at the source level. An optional DEBUG EPROM is available which will work with Paradigm's Debug/RT Version 3.0 or later. The baud rate for the DEBUG EPROM is set to 38400 baud. Connect the serial I/O (tx and rx) from the Emulator PCA to either Com1 or Com2 on a PC. Operate Turbo Debug in the remote mode by entering the following at the DOS prompt:

>td -rs2 -rp*n progname*

where *progname* is the .exe file name to be debugged and *n* specifies the com port. The program must be compiled with debug options ON. The -rs2 sets the baud rate to be compatible with the

DEBUG EPROM. Refer to the Paradigm Debug/RT documentation for information on running the Paradigm debugger.

7. SERVICE

This section presents information for troubleshooting and repair of the 91050-60001 MAC DISK EMULATOR PCA. **Figure 5 - BKR 91060-60001 PCA Component Locations** presents the component arrangement on the PCA. **Figure 6 - BKR 91060-60001 Logic Diagrams** provides the logic diagrams for the MAC DISK EMULATOR PCA.

7.1. DIAGNOSTICS

LEDs are provided on the MAC DISK EMULATOR PCA for display of diagnostic information during power up and operation. Refer to the EMULATOR OPERATION section of this manual for information on the LED states and meanings.

7.2. LOGIC DIAGRAMS

Logic diagrams and wiring information for the PCA, Cable and Control Panel are provided in APPENDIX A.

8. REPLACEMENT PARTS

This section provides information necessary for parts replacement for the 91060A MAC DISK EMULATOR PCA. Table 15 - 91060-60001 Material List provides a list of replaceable parts along with a typical manufacturer and manufacturers part number. Parts may be obtained from local suppliers or manufacturer's distributor as required. Alternate manufacturers may be substituted for suppliers where alternate exact replacement parts are available.

CAUTION

The 91060-60001 MAC DISK EMULATOR PCA uses parts which are sensitive to STATIC discharge. Precaution must be taken when handling and replacing parts to assure protection of components from static discharge. As such, the 91060-60001 must only be handled by personnel familiar with ESD static protection methods. Caution must also be observed when shipping the assembly and during parts removal and replacement.

9. APPENDIX A

9.1. I/O ADDRESS ASSIGNMENTS

TABLE 10 - CONTROL AND STATUS I/O ADDRESSES

I/O ADDRESS (HEX)	ASSIGNMENT
8000 - Read	Read DIP Switch
8000 - Write	Write LEDs
8001 - Read	8-bit data input from P2
8001 - Write	8-bit data output to P2
8002 - Read	Backplane Status Register
8002 - Write	Buffer Control Register
8003 - Read	Buffer Status Register
8003 - Write	Backplane Control Register
803x	NCR 53C90A SCSI Controller Base Address

TABLE 11 - BACKPLANE CONTROL REGISTER BIT ASSIGNMENTS

Bit	Address = 8003 (Write)
0	Clear Flag
1	Set Flag
2	
3	
4	Clear Control F/F
5	Clear Command F/F
6	
7	Busy

APPENDIX A

TABLE 12 - BACKPLANE STATUS BIT ASSIGNMENTS

Bit	Address = 8003 (Read)
0	WRITE Buffer Input Address Bit 0
1	WRITE Buffer Input Address Bit 1
2	WRITE Buffer Output Address Bit 0
3	WRITE Buffer Output Address Bit 1
4	READ Buffer Input Address Bit 0
5	READ Buffer Input Address Bit 1
6	READ Buffer Output Address Bit 0
7	READ Buffer Output Address Bit 1

TABLE 13 - BUFFER STATUS BIT ASSIGNEMENTS

Bit	Address = 8002 (Read)
0	READ BUFFER not empty
1	READ BUFFER full
2	WRITE BUFFER not empty
3	WRITE BUFFER full
4	Command F/F Status
5	Control F/F Status
6	Flag F/F Status

TABLE 14 - BUFFER CONTROL BIT ASSIGNMENTS

Bit	Address = 8002 (Write)
0	Enable WRITE DMA
1	Enable READ DMA
2	
3	
4	
5	Reset WRITE Buffer Address
6	Reset READ Buffer Address
7	Reset EDT Status F/F

APPENDIX A

TABLE 15 - 91060-60001 MATERIAL LIST

Part Number	Description	Qty	Mfg	MFG P/N	Reference Des.
22-0010	FUSE, MICRO 1 AMP	1 EA	LITTLEFUSE	273001	F1
22-0022	SWITCH, DIP 8 POS.	1 EA	GRAYHILL	76-SB08S	U57
25-0015	HEADER, POST 96 PIN (3X32) .025 SQR	0.3 EA	3M/APT	929831-01-36	W1-W11
25-0057	SOCKET, I.C. PLCC 68 PIN	2 EA	AMP	821574-1	XA51, XA55
25-0058	SOCKET, I.C. 32 PIN .6 SPC	4 EA	T.I.	C8832-01	XA44-XA47
30-0010	RES., MET. FILM 3.32K OHM 1/4 W 1%	3 EA	IRC	RN55C3321F	R2,3, 4
30-0023	RES., MET. FILM 82.0K 1/4 W 1%	1 EA	ANY	RN55C8202	R1
30-0032	RES., PACK, SIP 1.5 KOHM 10 PIN 9 RES	9 EA	BOURNS	4610X-101-152	RP1-RP9
30-0034	RES., PACK, SIP 4.7K 10 PIN 9 RES	1 EA	BOURNS	4610X-101-332	RP12
30-0035	RES., PACK, SIP 110 10 PIN 9 RES	2 EA	BOURNS	4610X-101-111	RP10, 11
31-0003	CAP., MIN. ELCTRO. 22 UF 16V 20%	7 EA	MALLORY	VTL22S35	C3-C7, C58,C62
31-0004	CAP., MONOLITH CER 0.1 UF 50V	50 EA	MALLORY	CK05BX104M	C9-C55, C59-C61
31-0009	CAP., METAL. POLYSTR 0.1 UF 50V 10%	1 EA	MALLORY	168104J50A	C1
31-0010	CAP., MIN. ELECTR. 22 UF 25 V 20%	2 EA	SPRAUGE	513D226M050AA4	C56, 57
31-0012	CAP., MONOLITH CER .01 UF 100V	1 EA	AVX	SR211E103MAA	C2
34-0014	LED, RED, RECT	4 EA	ANY		DS1-4
36-0005	OSC, TTL TXCO 19.66 MHZ	1 EA	DALE	XO-43B-19.66	U49
40-0005	DIODE, SCHOTTKY 1 AMP 40V	1 EA	MOTOROLA	1N5818	D1
42-0004	IC, TTL LS 74LS14	1 EA	ANY	74LS14	U31
42-0006	IC, TTL LS 74LS244	4 EA	ANY	74LS244	U34, U36, U53, U56
42-0012	IC, H CMOS 74HC04	1 EA	ANY	74HC04	U50
42-0013	IC, ALS TTL 74ALS32	1 EA	ANY	74ALS32	U32
42-0016	IC, ALS TTL 74HCTS373	1 EA	ANY	74ALS373	U40
42-0017	IC, ALS TTL 74ALS374	4 EA	ANY	74ALS374	U16, U29, U52, U54

APPENDIX A

Part Number	Description	Qty	Mfg	MFG P/N	Reference Des.
42-0018	IC, ALS TTL 74ALS393	3 EA	ANY	74ALS393	.U18, U27, U38
42-0022	IC, ALS TTL 74ALS08	1 EA	ANY	74ALS08	.U17
42-0023	IC, ALS TTL 74LS139	1 EA	ANY	74ALS139	.U33
42-0026	IC, ALS TTL 74ALS245	1EA	ANY	74ALS245	.U41
42-0027	IC, LS TTL 74LS670	8 EA	ANY	74ALS670	.U19-U26
42-0030	IC, UPROCESSOR PD70208-10 (V40)	1 EA	NEC	PD70208-10	.U51
42-0031	IC, INTERFACE SN75121N	12 EA	ANY	SN75121N	.U4-U15
42-0035	IC, RS232 DRVR/RCVR LT1039	1 EA	LINEAR TECHNOLOGY	LT1039N-16	.U48
44-0004	IC, POWER SUPERV 5 V	1 EA	TI	TL-7705A	.U39
44-0005	IC, REGULATOR 2.85V	1 EA	TI	TL-SCSI285N	.U58
83-0009	PAL, PGMD MEMD20R4	1 EA	ATst SYSTEMS	83-0009	.U43
83-0010	PAL, PGMD SCSI20L8	1 EA	ATst SYSTEMS	83-0010	.U42
83-0011	PAL, PGMD FLGA20L8	1 EA	ATst SYSTEMS	83-0011	.U1
83-0012	PAL, PGMD FLGB20L8	1 EA	ATst SYSTEMS	83-0012	.U2
83-0013	PAL, PGMD BPIN16R4	1 EA	ATst SYSTEMS	83-0013	.U30
83-0014	PAL, PGMD BPOUT16R4	1 EA	ATst SYSTEMS	83-0014	.U37
83-0015	PAL, PGMD FIFS16L8	1 EA	ATst SYSTEMS	83-0015	.U35
83-0016	PAL, PGMD EDT16R4	1 EA	ATst SYSTEMS	83-0016	.U28
83-0017	PAL, PGMD CON20L8	1 EA	ATst SYSTEMS	83-0017	.U3